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THESIS

MEASURED NOISE PERFORMANCE OF A POST-DETECTION
LIMITER CIRCUIT IN THE RECEIVER
OF A BINARY DATA TRANSMISSION SYSTEM

by

William John Luk

March 1986

Thesis Advisor: G. A. Myers

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Measured Noise Performance of a Post-Detection Limiter Circuit in the Receiver of a Binary Data Transmission System

by

William John Luk
Captain, United States Army
B.S., United States Military Academy, 1976

Submitted in partial fulfillment of the
requirements for the degree of

MASTER OF SCIENCE IN ELECTRICAL ENGINEERING

from the

NAVAL POSTGRADUATE SCHOOL
March 1986

ABSTRACT

Binary phase shift keying is a common modulation method for transmitting binary data because of its superior noise performance. A proposed alternative to the common BPSK receiver is use of three parallel post-detection circuits and majority decision logic to reduce errors, improving the overall performance of the BPSK system. The noise performance of each of two parallel circuits was measured and compared. The first circuit is a conventional BPSK receiver using an integrate and dump circuit. The second circuit incorporates a limiter after the demodulator and prior to the integrate and dump circuit. The conventional circuit is found to provide the same error probability at a 0.2 dB smaller signal to noise ratio. The probability density function of the voltage at various nodes in the post-detection circuits are measured and included in the report along with curves of probability of error versus SNR for the two post-detection circuits.

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TABLE OF SYMBOLS AND ABBREVIATIONS

AVM	Analog Voltage Multiplier
BPSK	Binary Phase Shift Keying
BW	Bandwidth
$c(t)$	Bipolar Data
C	Correlation
$d(t)$	Unipolar Output of Data Source
$d_1(t)$	Experimental Data Recovered in Non-limiter Circuit
$d_2(t)$	Experimental Data Recovered in Limiter Circuit
D	Number of Errors Made by $\overline{L}$ Circuit and not by L Circuit
E	Number of Errors Made by L Circuit and not by $\overline{L}$ Circuit
E_b	Bit Energy for One Bit Duration
f_c	Center Frequency of Bandpass Filter
f_1	Lower -3dB Frequency of Bandpass Filter
f_u	Upper -3dB Frequency of Bandpass Filter
FSR	Feedback Shift Register
GIC	Generalized Immitance Converter
L	Limiter
$\overline{L}$	Non-Limiter
$n(t)$	Noise Time Waveform
N	Average Noise Power Measured at the Input to the Demodulator
N_c	Number of Errors Made by Both L and $\overline{L}$ Circuits on the Same Bit
N_L	Number of Errors from the L Circuit
$N_{\overline{L}}$	Number of Errors from the $\overline{L}$ Circuit
N_o	Magnitude of Spectral Density Function of the Noise

PDF	Probability Density Function
PE	Probability of Error
R	Resistive Component of Impedance Across the True RMS Voltmeter
Rq	Variable Resistor used to Set Q of the Bandpass Filter
s(t)	BPSK Output
S	Average Signal Power Measured at the Input to the Demodulator
SNR	Signal to Noise Ratio
(t_1, t_2)	Bit Interval Starting at Time t_1 and Ending at Time t_2
T	Bit Period
TTL	Transistor-Transistor Logic
V_1	RMS Voltage of Signal Time Waveform
V_2	RMS Voltage of Signal Plus Noise Time Waveforms
y(t)	BPSK Signal Plus Noise Time Waveform

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I. INTRODUCTION

A. BACKGROUND

Binary phase shift keying (BPSK) is a common signaling method for transmission of binary data because of its superior noise performance. A typical BPSK signal is shown in Fig. 1-1, where T equals the bit period. (Although Fig. 1-1 depicts the data synchronized with the zero crossings of the carrier, the actual phase of the carrier when the reversal occurs changes from bit to bit). The performance of BPSK with Additive White Gaussian Noise (AWGN) has been mathematically

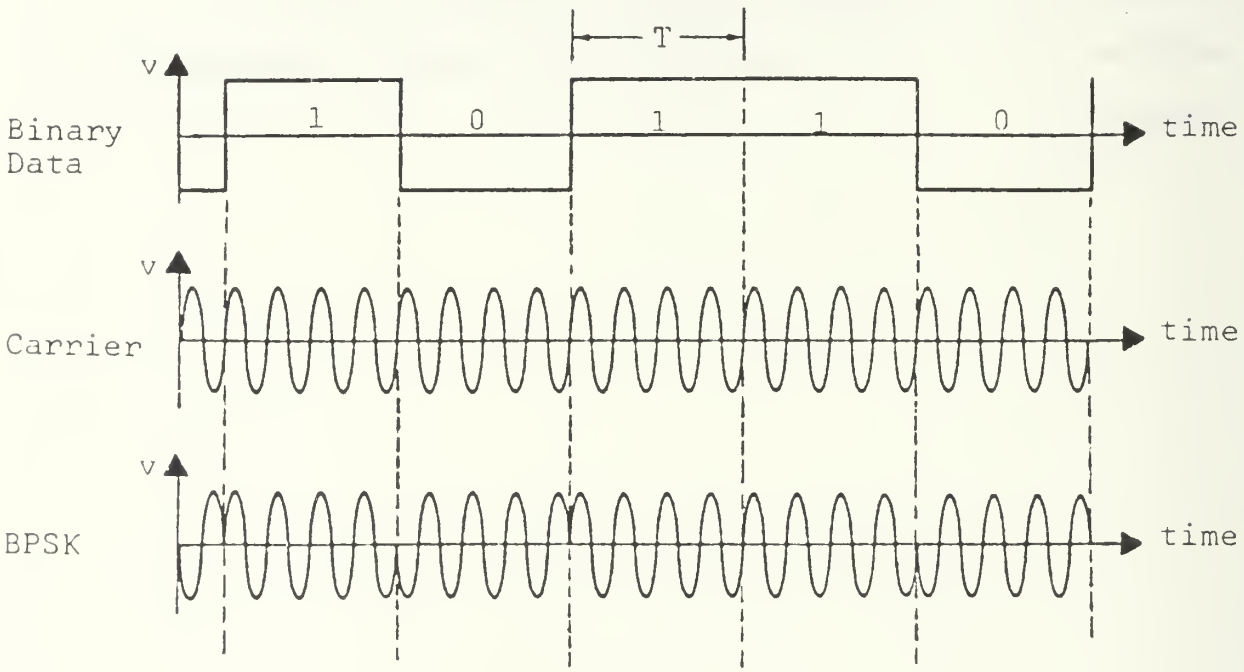


Fig. 1-1. Typical BPSK Waveform.

derived and is expressed in terms of probability of error (PE) for a given E_b/N_o. E_b is the bit energy for one bit period, and N_o is the magnitude of the spectral density function of the noise. A typical BPSK performance curve is presented in Fig. 1-2 [Ref. 1: p. 159]. Probability of error for a digital communication system is a ratio of the number of bits received in error to the total number of bits received. Since it is impossible to measure bit energy within the receiver circuit, E_b/N_o is expressed as a signal to noise (SNR) ratio, where S is the average signal power measured at the input to the demodulator and N is the average noise power. The typical BPSK performance curve models noise as a random variable with a Gaussian distribution. As such, the bandpass noise experiences random frequency and amplitude variations with time. It is these time variations of frequency and amplitude which this research investigates with the intent to improve the overall performance of the BPSK system.

B. OBJECTIVE

The objective of this thesis is to investigate a means of decreasing the probability of error for a given SNR in a BPSK system. Two parallel post-detection receiver circuits are implemented in an effort to exploit a particular characteristic of the received random voltage.

C. PROCEDURE

The first stage of the experiment is constructing the transmitter which is composed of a data source and a modulator. Next, a noise summing circuit representing the channel is built. The front end of

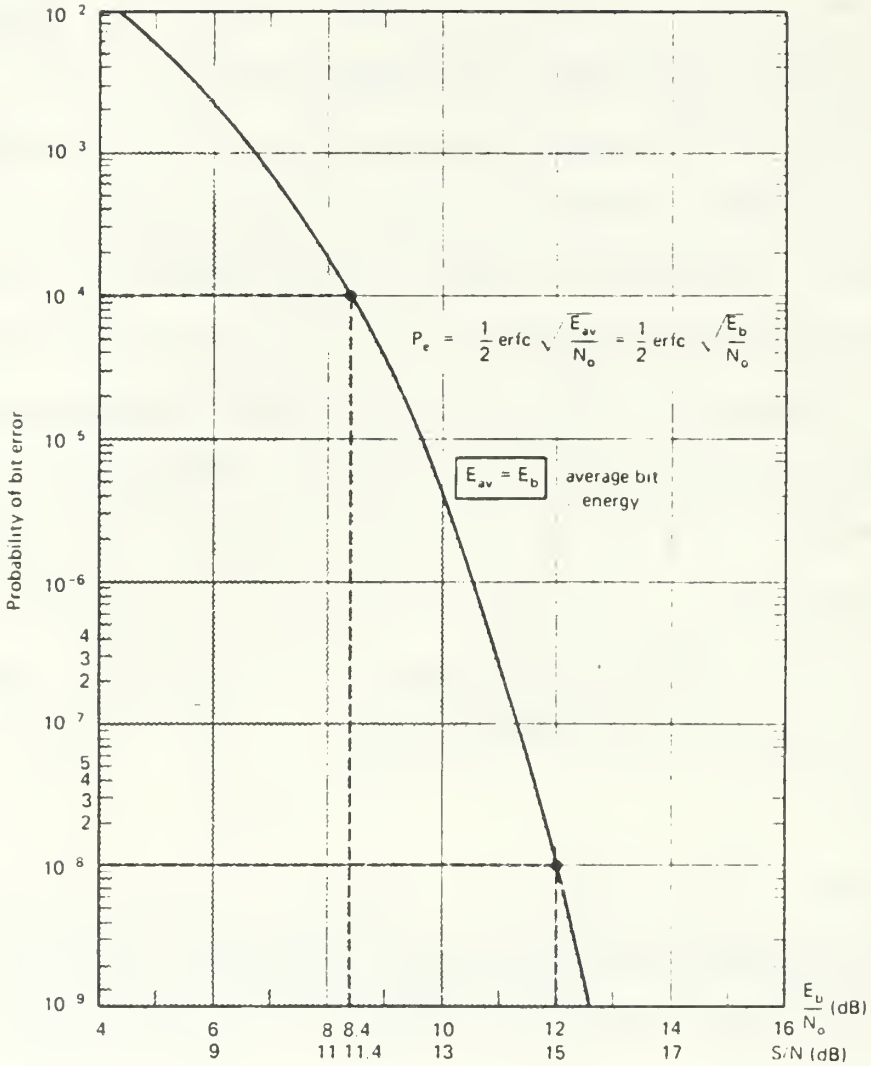


Fig. 1-2. PE vs E_b/N_o for BPSK Signaling.

the receiver is composed of a bandpass filter and a demodulator. The signal after demodulation enters an integrate and dump circuit. In this paper we refer to this typical system as the ($\overline{L}$) non-limiter circuit. In this research, a second channel, (L), similar to the first, except that an RC filter and a hard limiter precede the integrate and dump, is built and tested. Each receiver circuit had its own error detector circuit and digital counter. Once the entire system is working, the number of errors is measured for various SNR and probability of error is calculated. Probability density functions of the integrate and dump and sample and hold outputs verify the correct operation of the circuit.

D. SUMMARY OF RESULTS

The results of the experiment obtain and compare data of the typical BPSK system (Fig. 1-2) as obtained mathematically, d(t), with the two experimental data sets: $d_1(t)$ from the $\overline{L}$ circuit and $d_2(t)$ from the L circuit. The results show that:

1. The PE versus SNR curve for $d_1(t)$ is about 3 to 4 dB better than d(t), as expected due to the bandwidth of the bandpass filter.

2. The PE versus SNR curve for $d_1(t)$ is about 0.2 dB better than that for $d_2(t)$ for all SNR ratios.[1] The $\overline{L}$ circuit performs slightly better than the L circuit for all values of SNR.

3. The errors can be classified into three categories: a) limiter unique errors, b) non-limiter unique errors, and c) common errors. The limiter errors occur most often for a given SNR, followed by the common error, and then the non-limiter error. For small values of SNR, it was found that 50% of the errors made are common errors (an error made by both the L and $\overline{L}$ circuit on the same bit), where the other half of the errors made by either L circuit or $\overline{L}$ circuit.

E. CONTENTS OF THE REPORT

The experimental system as constructed is presented, along with photographs of the actual waveforms at different points in the circuit, in Chapter II. The L and $\overline{L}$ circuits are presented in this chapter. Chapter III indicates the performance of the L and $\overline{L}$ circuits when noise is added to the system. Next, the results of the experiment are presented in Chapter IV, with an analysis of the L unique, $\overline{L}$ unique, and common errors, and of the performance curves. Finally, conclusions are presented in Chapter V along with specific recommendations for future work on this research area.

II. THE EXPERIMENTAL SYSTEM

A. GENERAL

The experimental system is composed of the transmitter, channel, receiver, error detector, and timing subsystems as shown in Fig. 2-1. A BPSK signal s(t) is transmitted through the channel where noise n(t) is added. The BPSK signal plus noise time waveform y(t) is demodulated in the receiver and the data d(t) is recovered. The error detection circuit then counts the received bits which are in error. The timing system synchronizes the receiver, transmitter, and error detector. Circuit diagrams for each subsystem are shown in Figs. A-1 to A-9 in the Appendix.

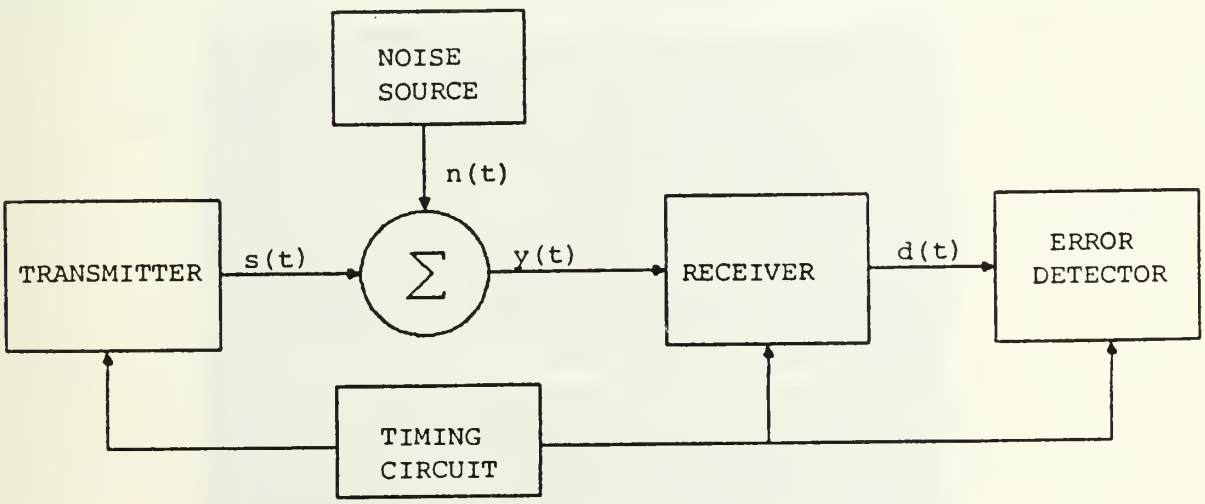


Fig. 2-1. The Experimental System.

B. SUBSYSTEMS

1. Transmitter

The transmitter is composed of a data source and modulator to produce a BPSK output (see Fig. 2-2). The data source uses a feedback shift register (FSR) to generate a repeating m-sequence for a random binary data source. The data d(t) is converted from unipolar TTL levels to a bipolar signal, c(t). The data then modulates a sinusoidal carrier using an analog voltage multiplier to produce the BPSK waveform.

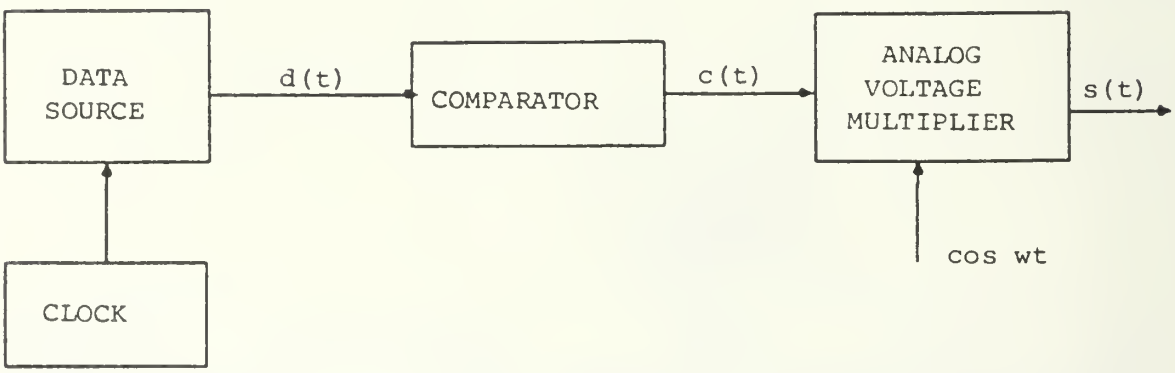
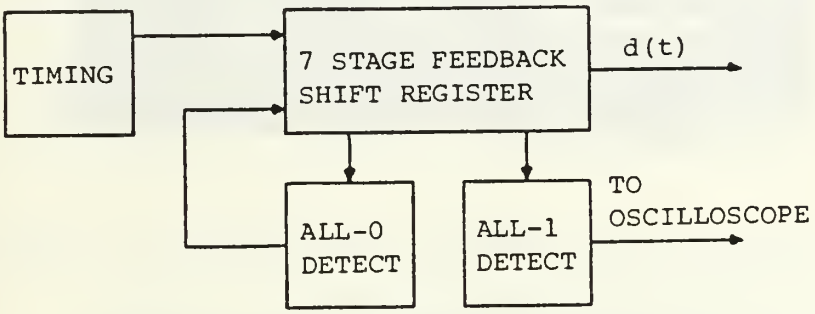


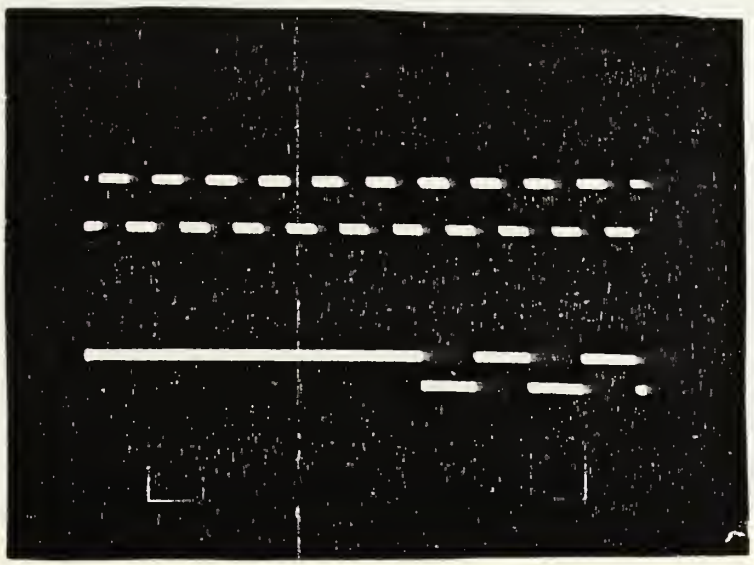
Fig. 2-2. The Transmitter Subsystem.

a. Data Source

A seven stage feedback shift register generates a repeating m-sequence of length $2^7 - 1 = 127$ bits per period as shown in Fig. 2-3a. It is constructed with D flip flops wired serially with feedback from taps 1 and 7 applied to an XOR gate. A 1 kHz clock drives the FSR. A circuit which applies a 1 to the FSR if the all-zero condition occurs is constructed. The all-one detect circuit provides a trigger pulse for the oscilloscope. The bit period is 1 millisecond.



(a)

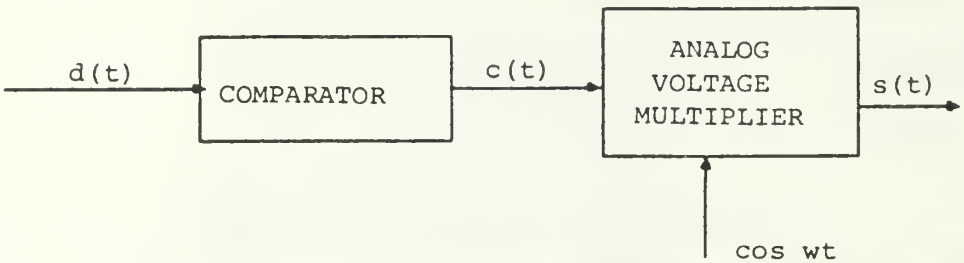


(b)

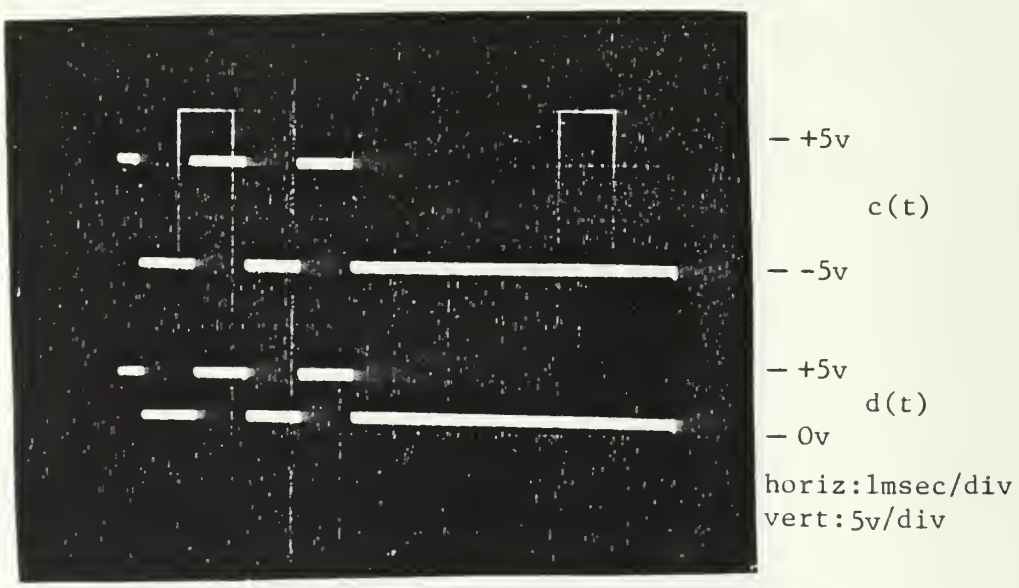
Fig. 2-3. Data Source Block Diagram (a) and Waveforms (b).

b. Modulator

The data d(t), at a rate of 1 kbps, is converted from TTL levels (0 to +5 volts) to bipolar levels with an LM311 comparator as seen in Fig. 2-4a. Fig. 2-4b shows the input bipolar data c(t) and the unipolar data d(t). The bipolar output, c(t) is multiplied by a sinusoid with frequency of 50 kHz to generate the BPSK output, s(t) where $s(t) = +A\cos(2\cdot\pi\cdot 50\cdot 10^{3})t$. Fig. 2-5a illustrates the BPSK waveform on a 1 to 0 transition. Fig. 2-5b shows the constant amplitude envelope of the BPSK waveform.



(a)



(b)

Fig. 2-4. Modulator Block Diagram (a) and Data Waveforms (b).

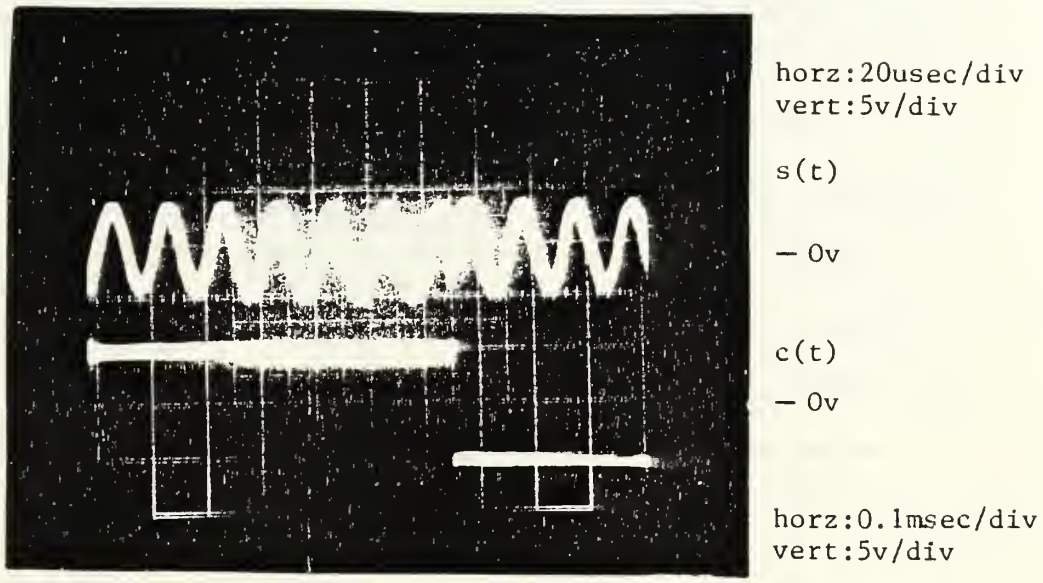


Fig. 2-5a. BPSK Waveform Showing a 1 to 0 Transition.

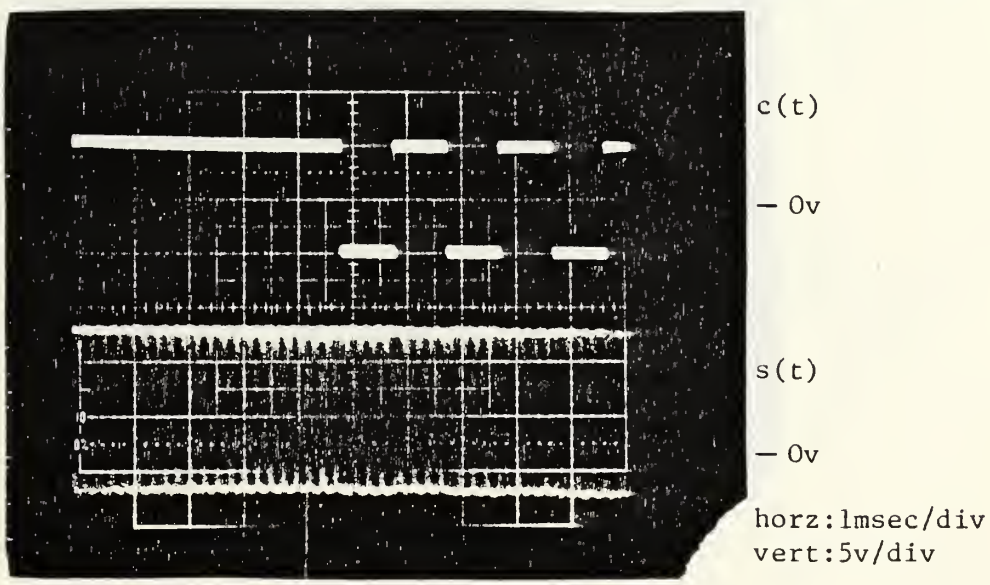
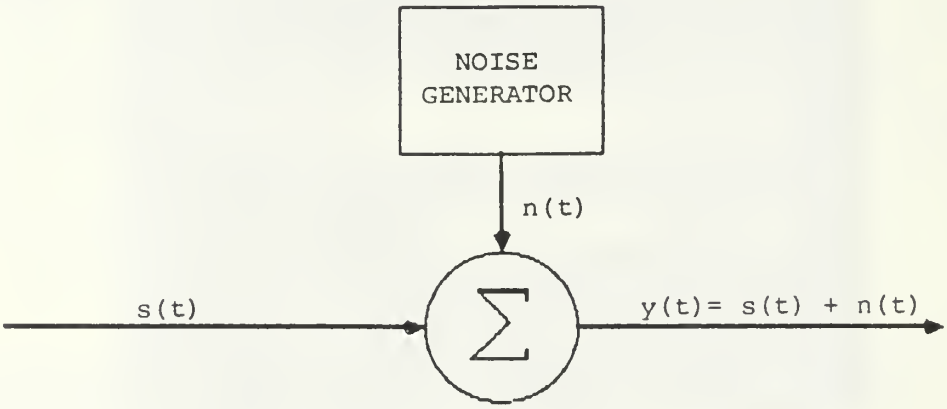


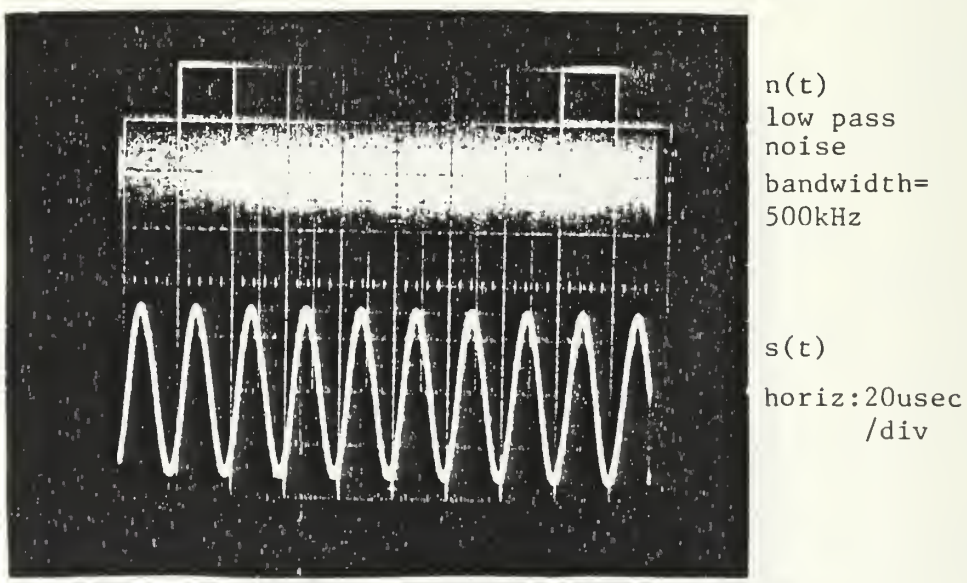
Fig. 2-5b. BPSK Waveform Showing the Constant Amplitude Envelope.

2. Channel

The effect of the channel (signal attenuation to the level of system noise) is created by adding noise n(t) to the transmitted signal s(t). An op-amp summing circuit is used as shown in Fig. 2-6.



(a)



(b)

Fig. 2-6. Channel Representation (a) and Waveforms (b).

3. Receiver

The signal plus noise voltage is applied to a bandpass filter in the receiver. The bandpass filter characteristic simulates the intermediate frequency amplifier in a typical superheterodyne receiver. The rest of the receiver consists of a demodulator and two post-detection circuits as shown in Fig. 2-7. A conventional post-detection circuit is called $\bar{L}$ in this report and has output $d_1(t)$. A second circuit called L incorporates a hard limiter and has an output $d_2(t)$. The objective of this research is to obtain and compare $d_1(t)$ with $d(t)$, $d_2(t)$ with $d(t)$, and $d_1(t)$ with $d_2(t)$.

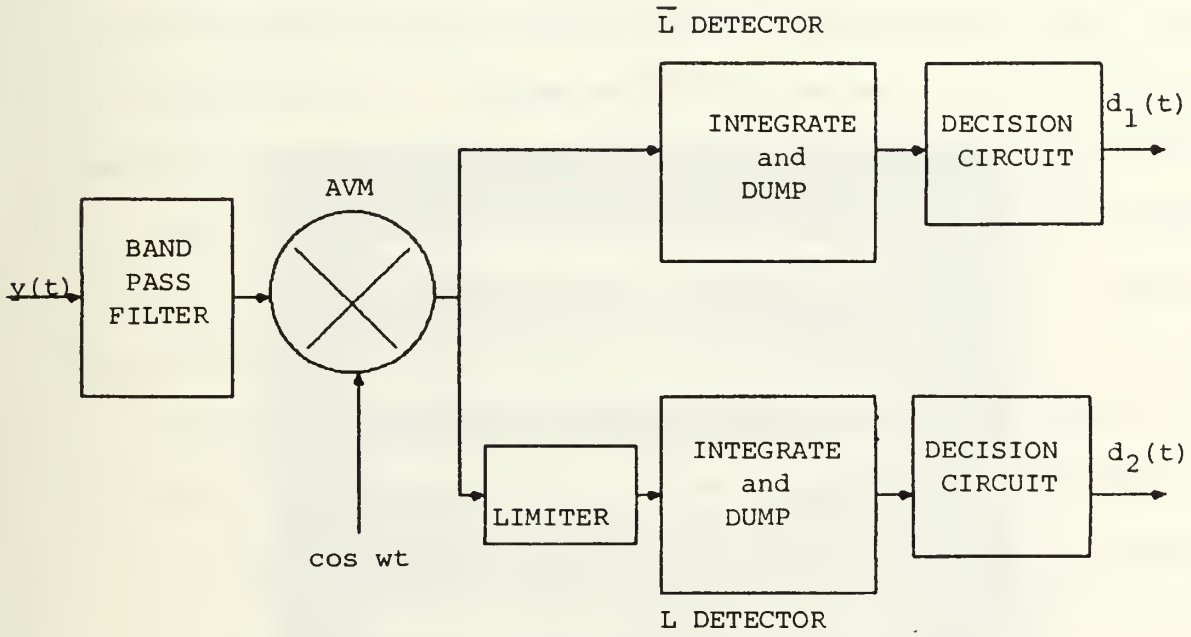


Fig. 2-7. Phase Detector Block Diagram.

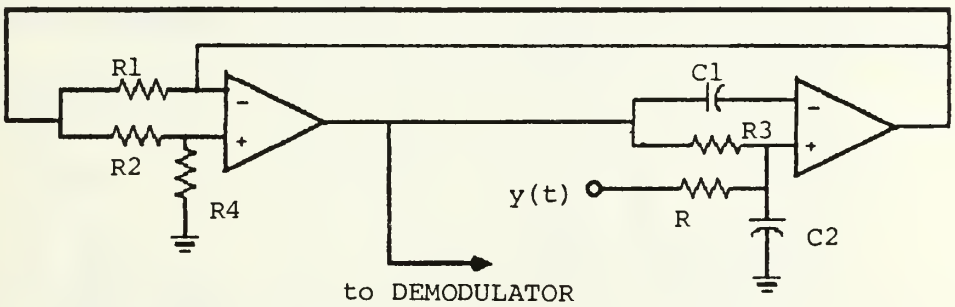
The receiver portion of Fig. 2-7 is realized as follows: the receiver consists of two channels; L and $\overline{L}$. The $\overline{L}$ channel represents a typical BPSK system. After demodulation, the signal plus noise voltage goes through a matched filter implemented by an integrate and dump circuit. The integrator is sampled at the end of each bit interval and the samples undergo a sign test in the decision device. If the sample is positive a binary "1" is decided, and if the sample is negative a binary "0" is decided. This estimate of the original data from the $\overline{L}$ circuit is called $d_1(t)$.

The second channel takes the demodulator output into an RC filter and a hard limiter prior to the integrate and dump. The RC filter recovers the DC component of the random voltage. Next, the hard limiter takes the DC output of the RC filter and either goes positive or negative to some designated level depending if the input signal is above or below the zero volt threshold. The L integrate and dump then reveals how often the waveform stays above or below the zero volt threshold. The L circuit determines how often the voltage is above or below the threshold. This is opposed to the $\overline{L}$ circuit which determines if the overall voltage in the bit interval is positive or negative, then using this information to decide. The experiment obtains and compares $d_1(t)$ with $d(t)$, $d_2(t)$ with $d(t)$, and $d_1(t)$ with $d_2(t)$.

a. Bandpass Filter

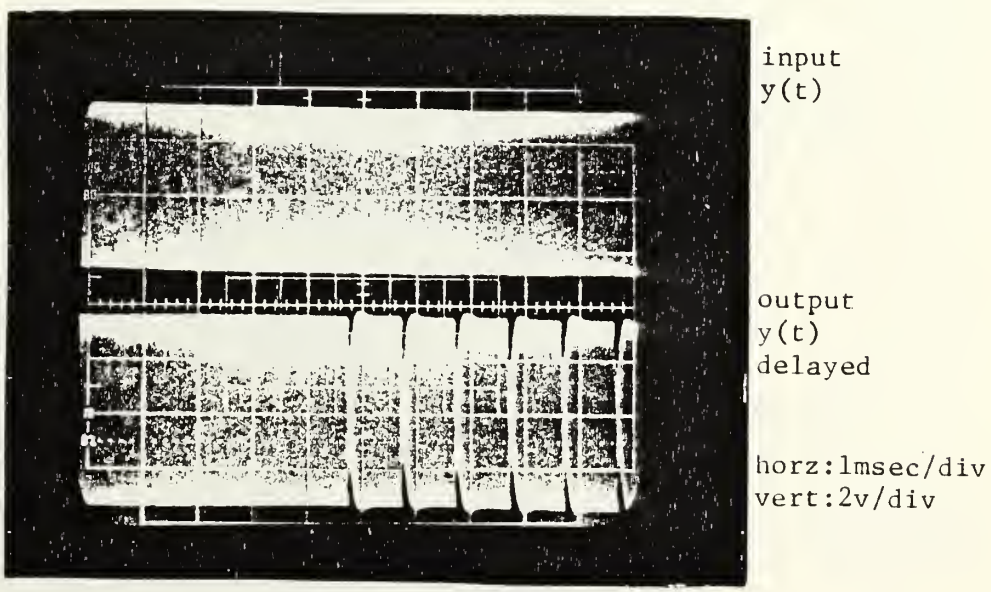
A Generalized Immittance Converter (GIC) configuration is chosen for the design of a bandpass filter with center frequency 50 kHz. This active filter shown in Fig. 2-8a has two operational amplifiers

and seven adjustable impedances which control the center frequency and bandwidth. The filter bandwidth is set to 2.94 kHz. The filter affects the amplitude of the signal plus noise as shown in Fig. 2-8b and also delays the waveform. The transfer function magnitude characteristics is shown in Fig. 2-9.



R1=R2=R3=R4=1k ohm
C1=C2=28 pf
R_q=17k ohm

(a)



(b)

Fig. 2-8. Bandpass Filter Block Diagram (a) and Waveforms (b).

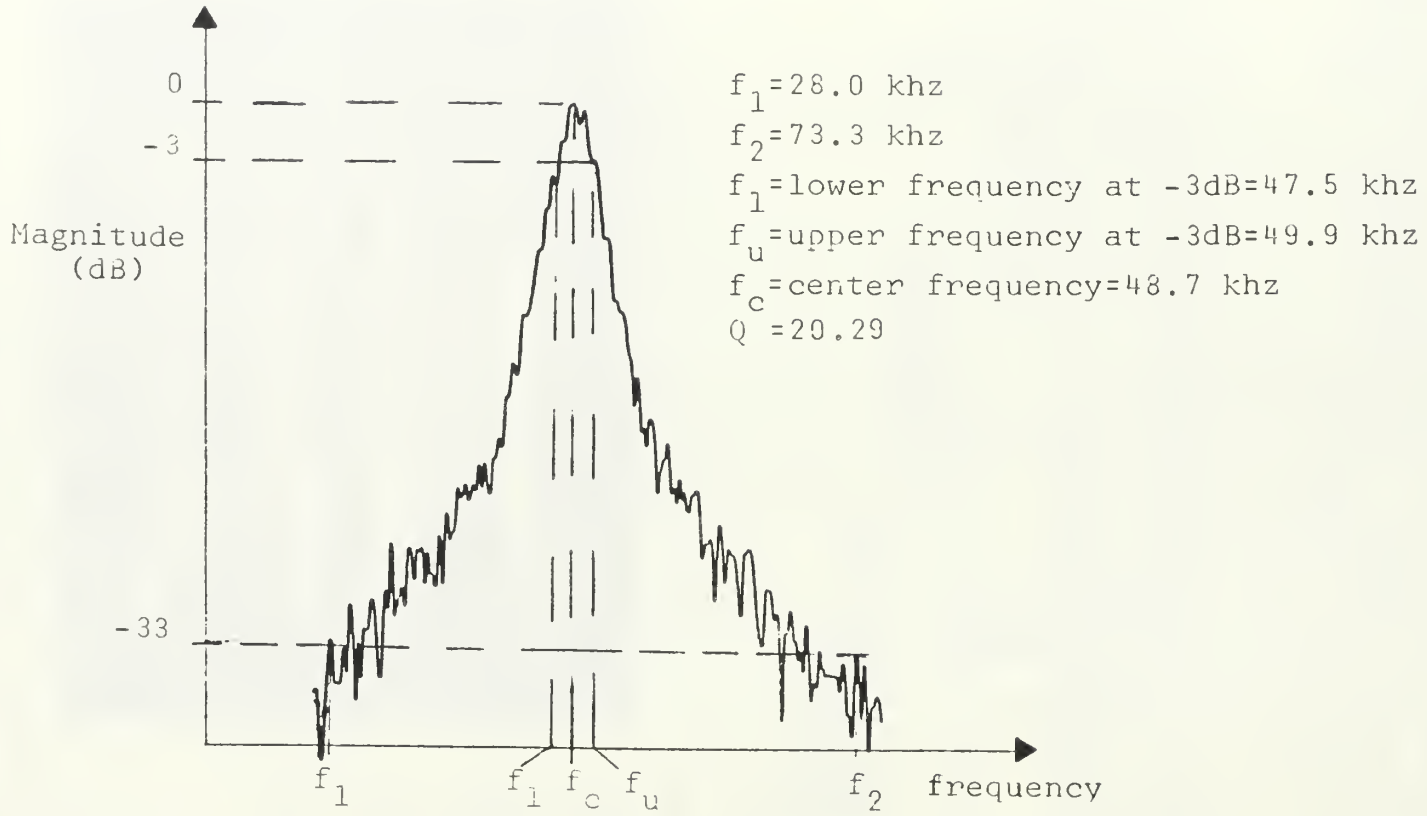
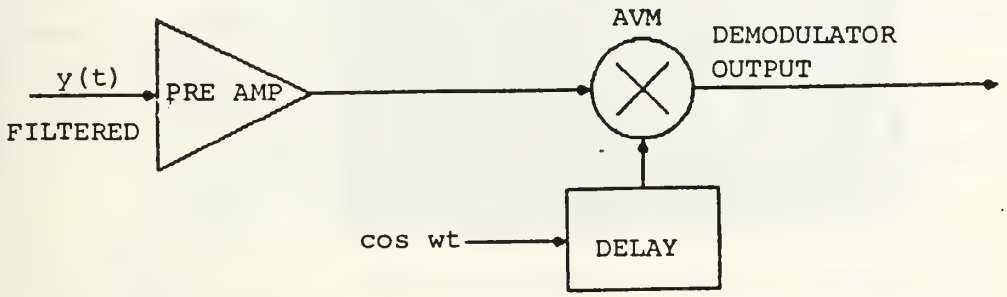


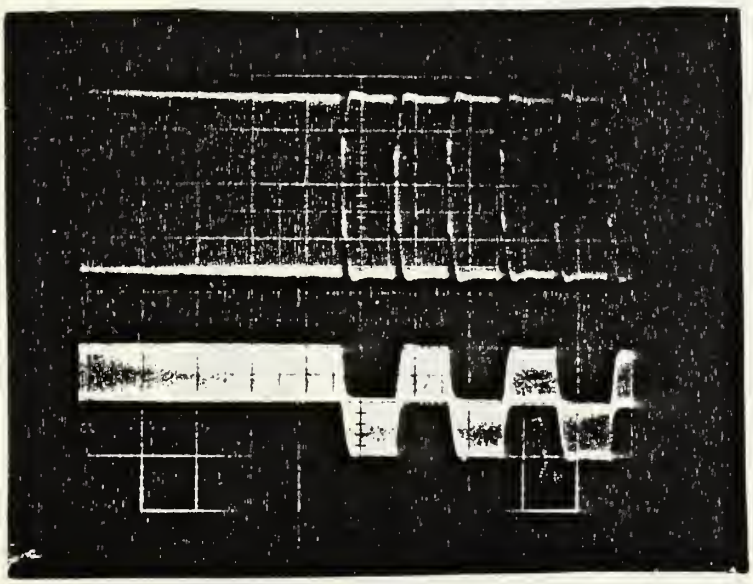
Fig. 2-9. Transfer Function of Bandpass Filter.

b. Demodulator

The demodulator is a coherent phase detector. A preamplifier (LM301) boosts the signal plus noise level after filtering. The sinusoid from the local oscillator is delayed for coherent demodulation to compensate for the delay caused by the bandpass filter. The output of the analog voltage multiplier is applied to both post-detection circuits, L and $\overline{L}$. The demodulator with waveforms is shown in Fig. 2-10.



(a)



(b)

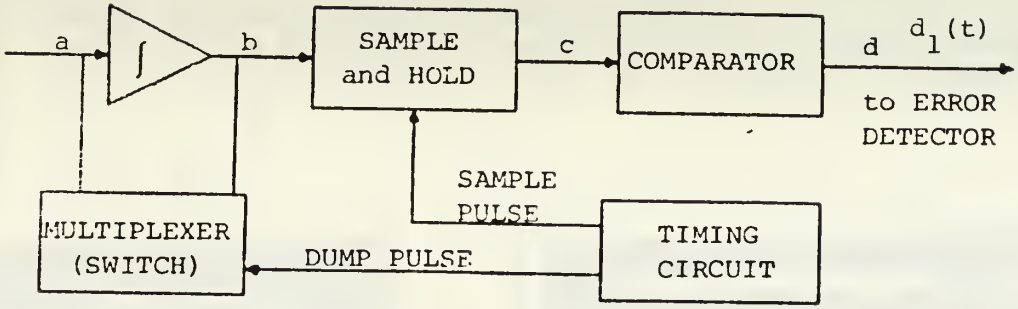
Fig. 2-10. Demodulator Block Diagram (a) and Waveforms (b).

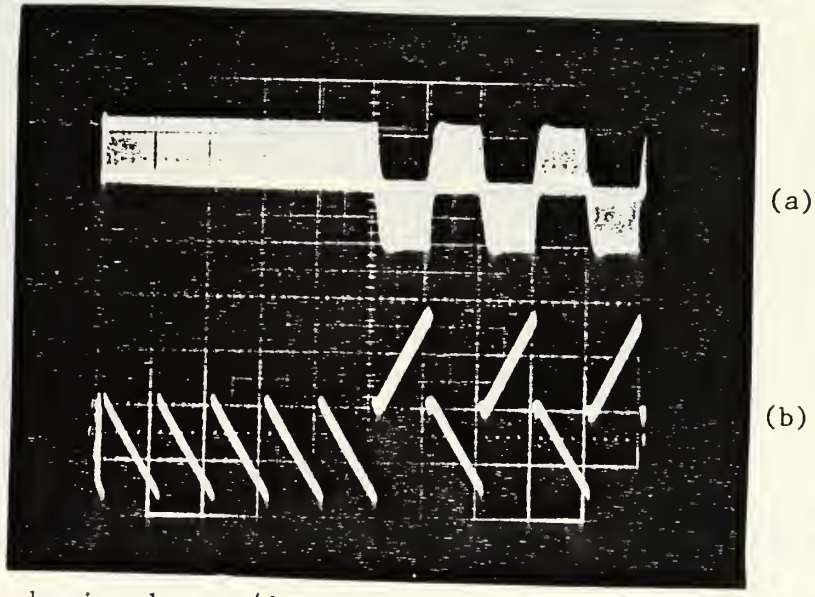
c. Non-Limiter ($\overline{L}$) Circuit

A block diagram and waveforms of the non-limiter ($\overline{L}$) circuit are shown in Fig. 2-11. The output of the demodulator enters the integrate and dump circuit where the signal plus noise voltage is integrated over the bit period. At the end of the bit period the integrator output is first sampled, then dumped. A comparator serves as the decision device and is set at the "zero" volt threshold. If the sample is positive, the comparator decides a "one" (plus five volts); if the sample is negative, a "zero" (zero volts) is decided. The output of the comparator is the recovered data, $d_1(t)$. The performance of the detector circuit is dependent on the accuracy of the timing system, which provides the sample pulse and dump pulse.

d. Limiter (L) Circuit

The limiter (L) circuit is presented in Fig. 2-12. The circuit is identical to the $\overline{L}$ detector, except an RC filter and a hard limiter precedes the integrate and dump. The RC filter eliminates the double frequency component of the demodulator output, leaving a lowpass waveform. The hard limiter characteristic is shown in Fig. 2-13. A positive voltage causes the limiter output to be a constant positive voltage. A negative voltage causes the limiter output to be a constant negative value. The integrate and dump, sample and hold, comparator, and timing system operate in the same manner as in the $\overline{L}$ detector. Notice that Fig. 2-12, part c, is the same as part f because there is no noise. The real value of the limiter operation occurs when noise is present.

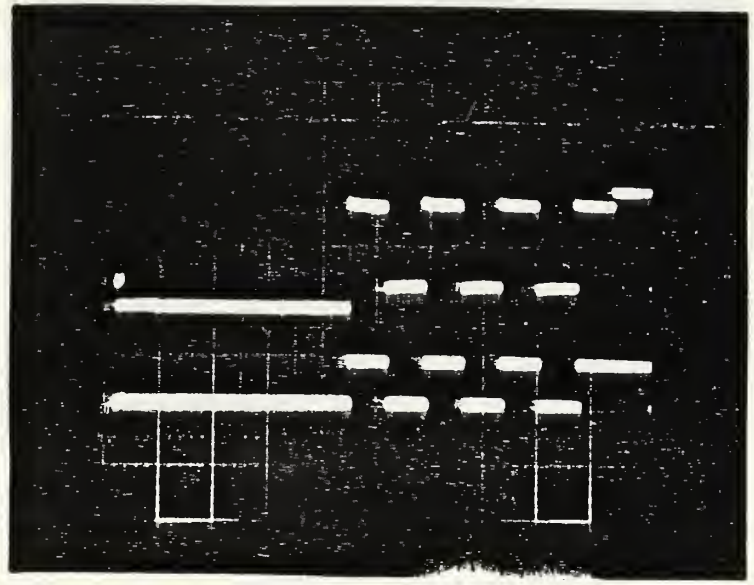




(a)

(b)

horiz: 1 msec/div vert: (a) 5 v/div
(b) 2 v/div

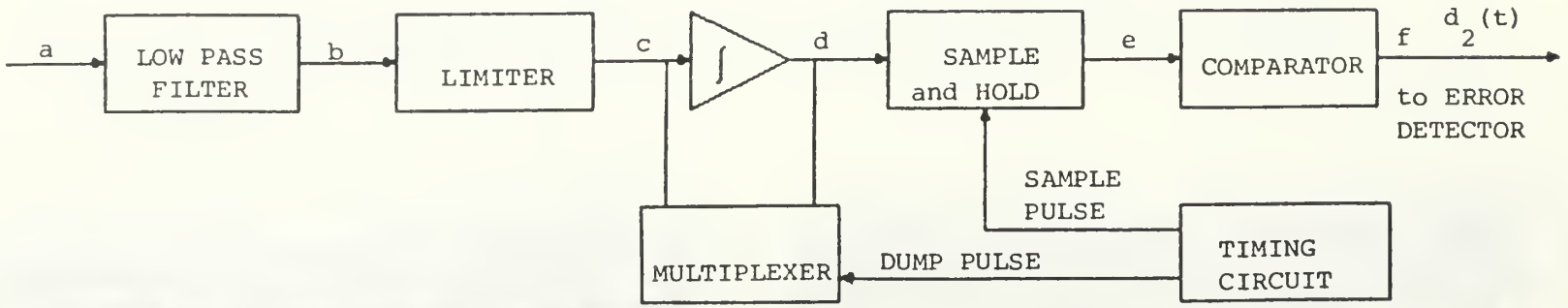


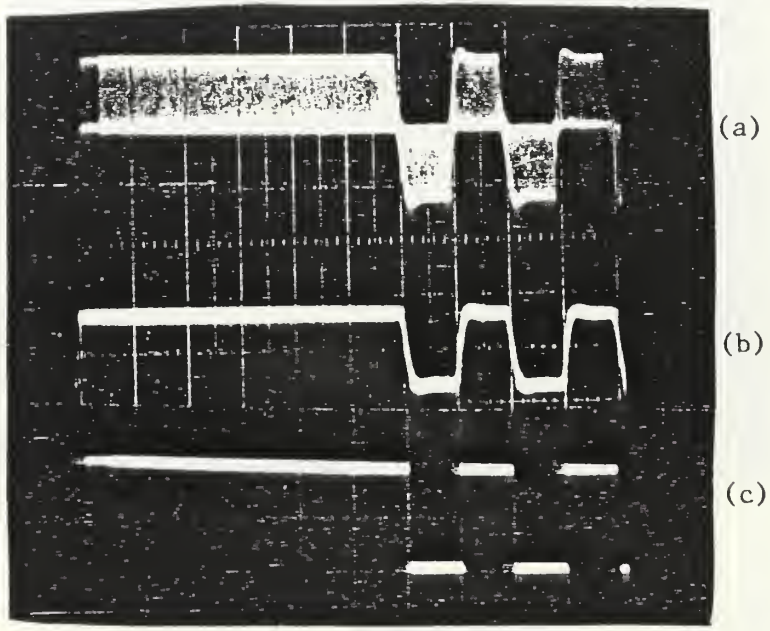
(c)

(d)

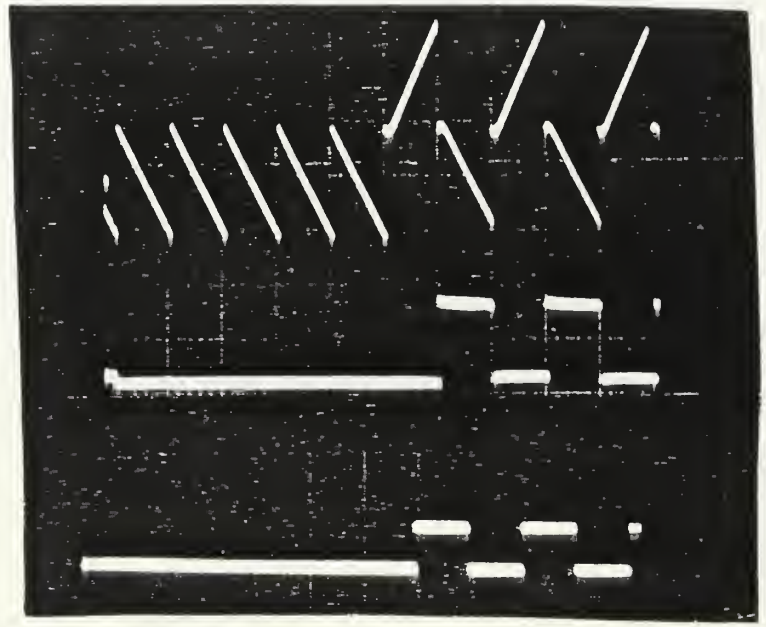
horiz: 1 msec/div Vert: 5v/div

Fig. 2-11. Non Limiter ($\overline{L}$) Circuit Block Diagram and Waveforms: a) Demodulator b) Integrate and Dump, c) Sample and Hold, d) Recovered Data $d_1(t)$.





horz: 1 msec/div vert: 5v/div



horz: 1 msec/div vert:(d,e)2v/div,(f)tv/div

Fig. 2-12. Limiter (L) Circuit Block Diagram and Waveforms: (a) Demodulator Output, (b) RC Filter Output, (c) Limiter Output, (d) Integrate and Dump, (e) Sample and Hold, (f) Recovered Data $d_2(t)$.

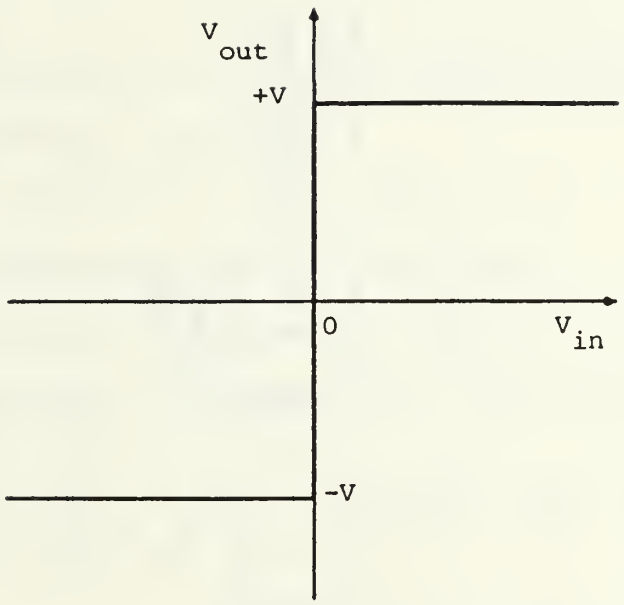


Fig. 2-13. Hard Limiter Input-Output Characteristic.

4. Error Detector

Estimates of the transmitted data, $d_1(t)$ and $d_2(t)$, are compared to the original data, d(t) bit by bit using the circuit of Fig. 2-14. This circuit compares the original and the recovered data by strobing these data at the middle of the bit interval. An error pulse is generated if the bits differ during the strobe pulse. With no noise, the original and recovered data are the same and no error pulses occur. The error pulses are conditioned by a Schmitt trigger to give a clean threshold level needed by the counters. Each of the L and $\overline{L}$ circuits has such an error detection circuit. Total bit count is obtained by counting the clock pulses from the timing system. This total bit count circuit is similar to the error detector circuit which is shown in Fig. 2-14.

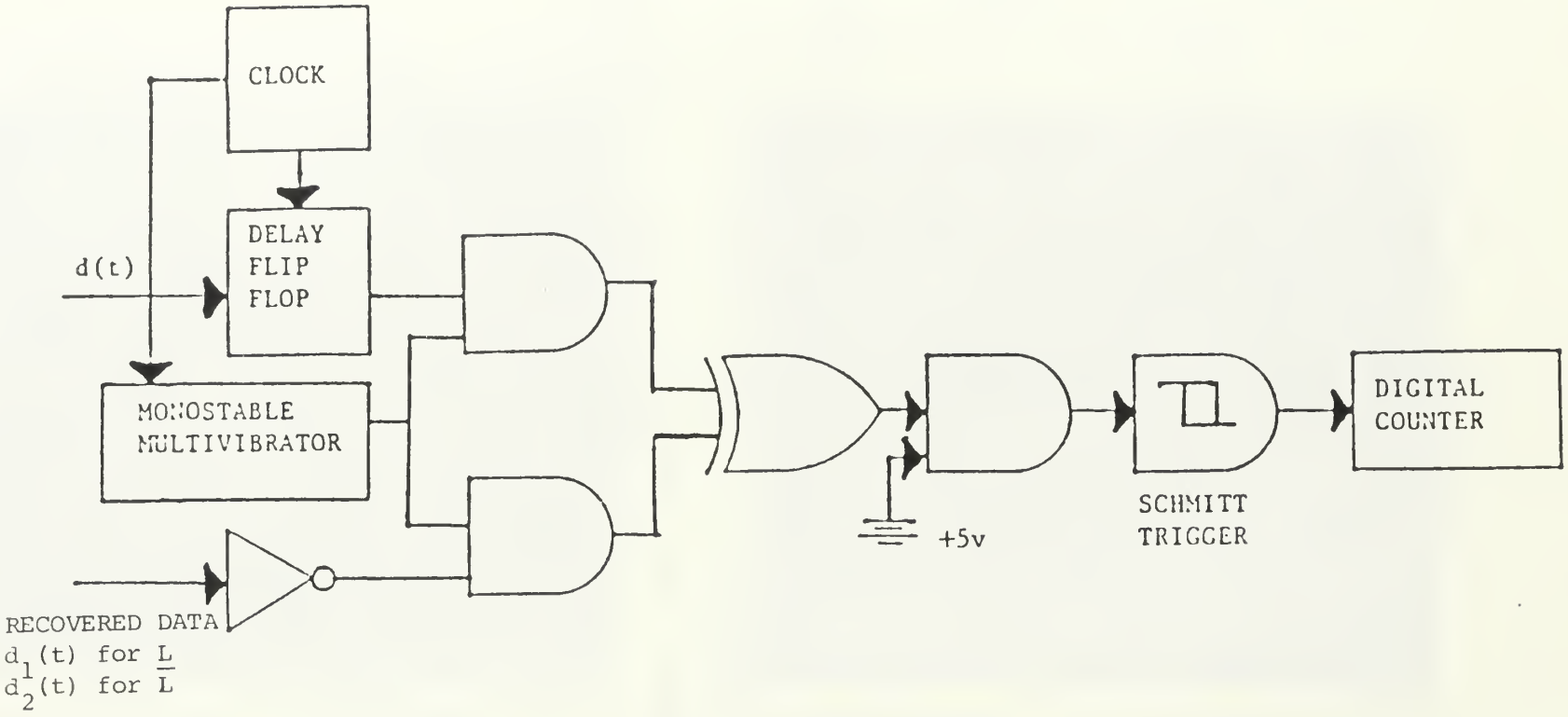


Fig. 2-14. Error Detector Circuit Used In Each of the Two (L and $\overline{L}$) Circuits.

5. Timing

One system clock, set a 1 kHz, provides timing for the following circuits illustrated in Fig. 2-15:

1. FSR - determines data rate of 1 kHz.
2. Integrate and dump - provides dump pulse.
3. Sample and hold - provides sample pulse.
4. Delay flip flop - synchronizes d(t), $d_1(t)$, $d_2(t)$ by providing a delay of one bit period.
5. Error detector - strobes d(t) and $d_1(t)$, d(t) and $d_2(t)$ at the middle of each bit interval to reveal errors. Common errors are detected in this same circuit.
6. Counter circuit - provides a total bit count during each experimental run directly from the clock waveform.

Timing diagrams for the experimental system is shown in Fig. 2-16. Observe that the sample pulse occurs in the last 10 microseconds of the bit period. The high to low transition of the sample pulse triggers the dump pulse which is also of length 10 microseconds. Therefore only a total of 20 microseconds is not used for integration during the 1,000 microsecond (1 millisecond) bit interval. The strobe pulse is used to compare the original and recovered data streams at the middle of each bit interval.

C. THE EXPERIMENTAL PROCEDURE

Several sets of data were taken to ensure the proper operation of the circuit. The method to collect data is:

1. Set the noise generator to 0 and record the signal level in rms volts as measured by a true rms voltmeter connected across the input to the demodulator.

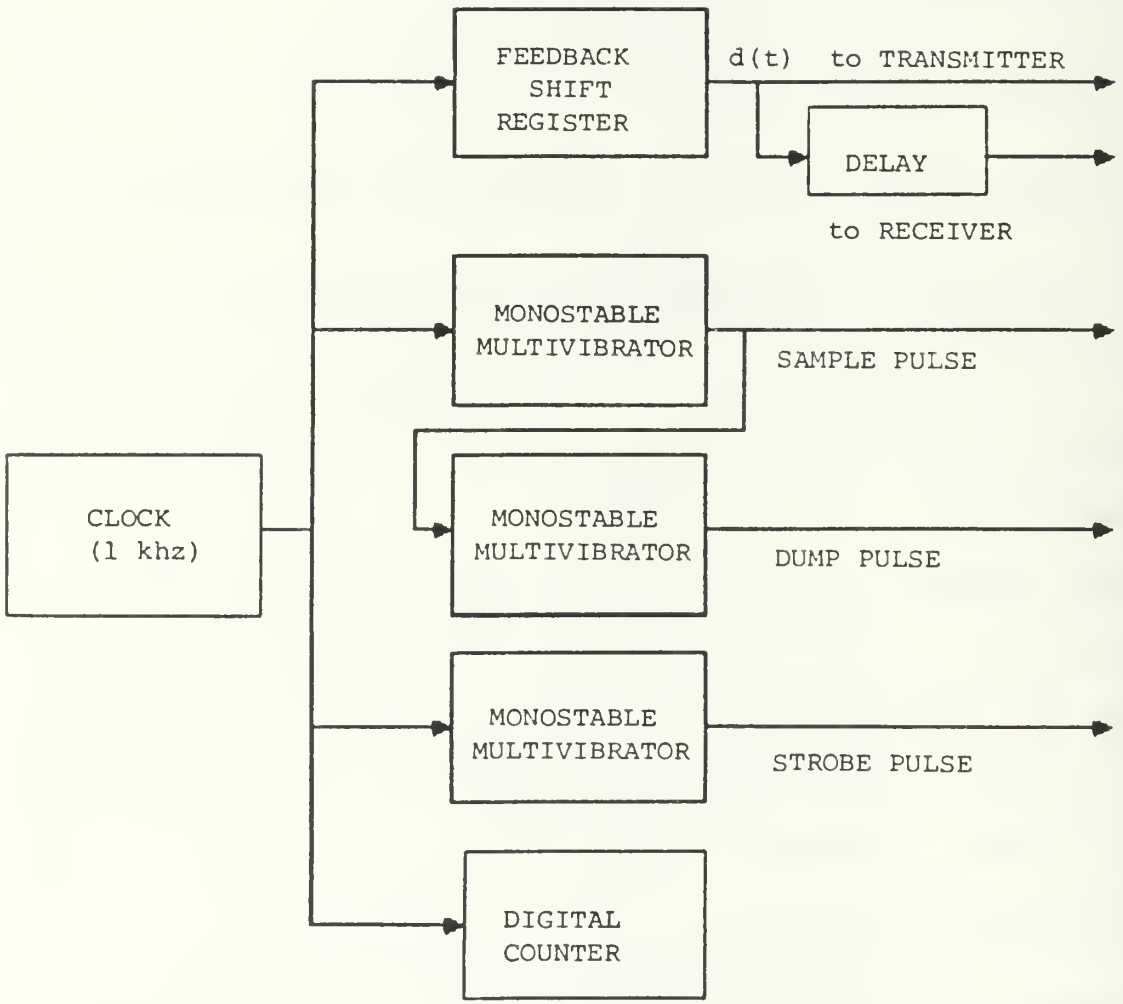
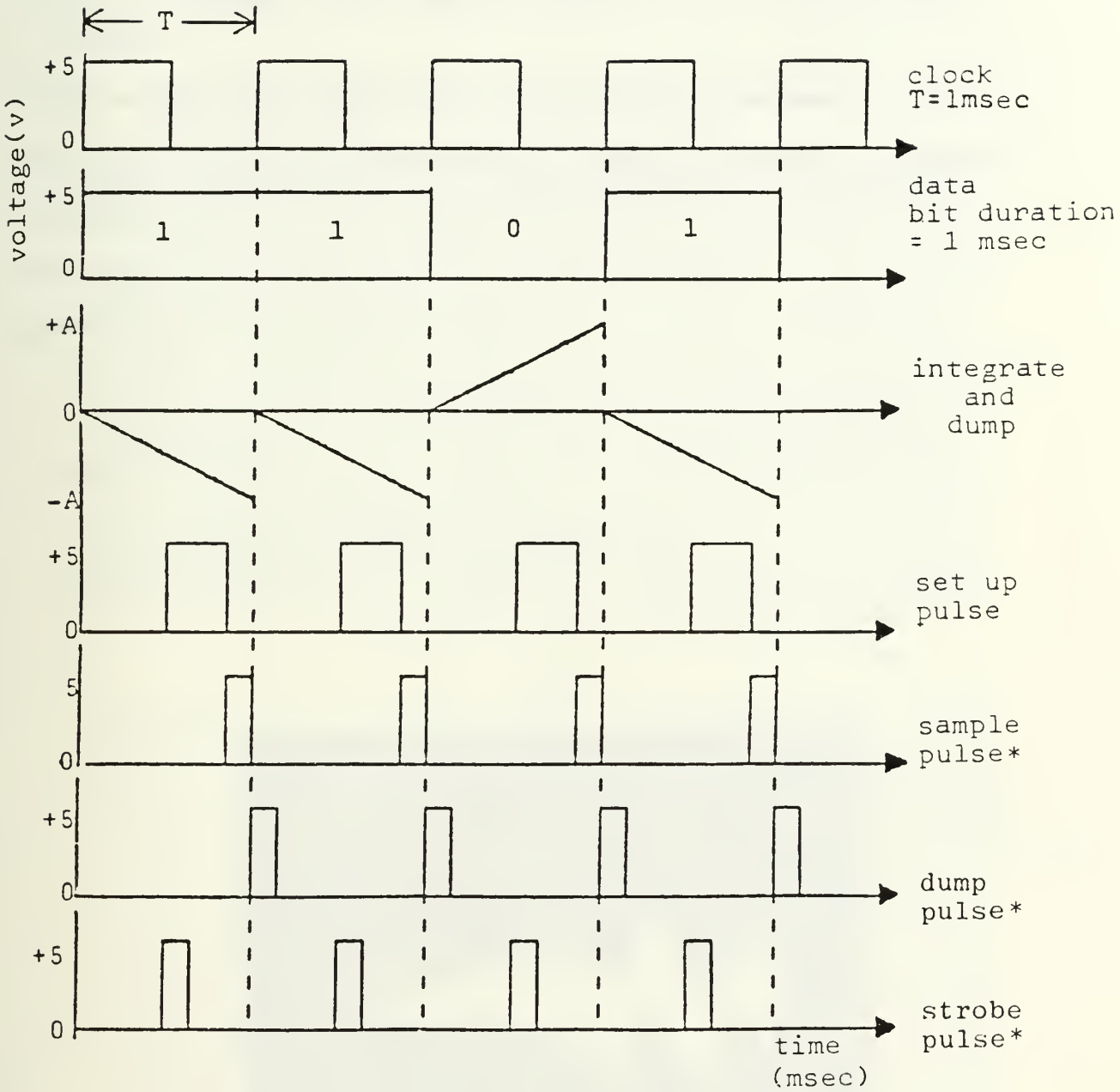


Fig. 2-15. Block Diagram of Timing Subsystem



*pulse width=10 usec

Fig. 2-16. Subsystem Timing Waveforms.

2. Increase the noise level and record the signal plus noise level in rms volts at the input to the demodulator.

3. Enable the gate which controls the data flow to the counters. The counters are wired to stop when the total bits transmitted is 2^{16} = 65,536 bits.

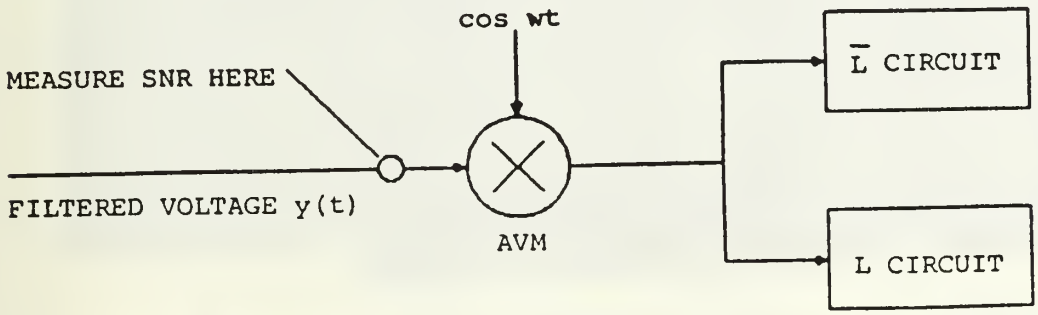
4. Record the number of errors on the L circuit, the $\bar{L}$ circuit, and the number of common errors directly from the digital counters.

5. Reset the counters, increase the noise level, and repeat steps 2 through 4 for a new value of SNR.

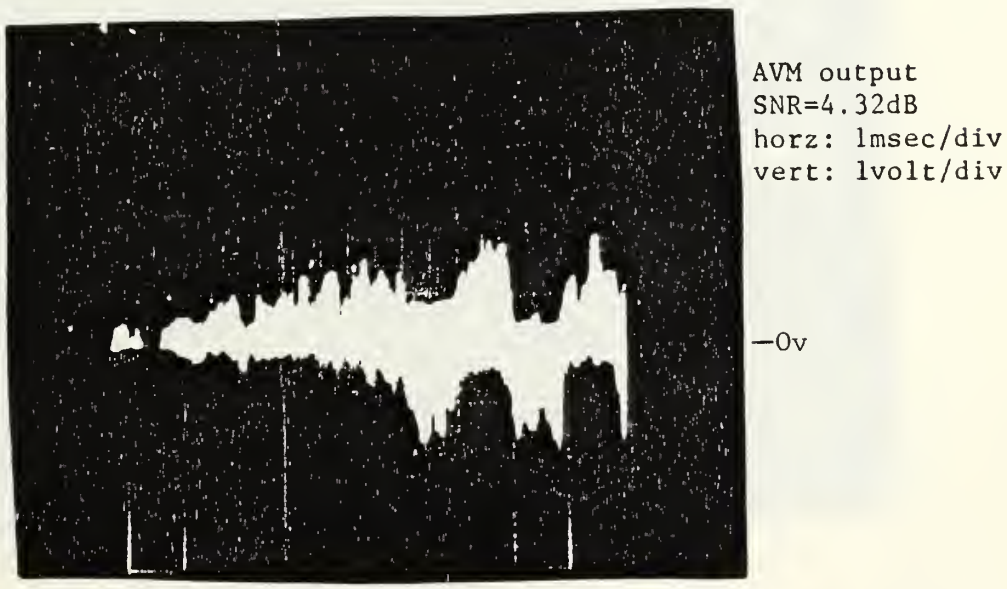
III. THE EXPERIMENTAL SYSTEM CHARACTERISTICS WITH NOISE

A. GENERAL

After the signal (BPSK) plus noise is bandpass filtered, it is applied to an analog voltage multiplier (AVM) for coherent demodulation as shown in Fig. 3-1a. The double frequency term (cos 100kHz), a $\pm$ DC level, and noise are all part of the output. This same output is now applied to both the L and $\overline{L}$ circuits.



(a)

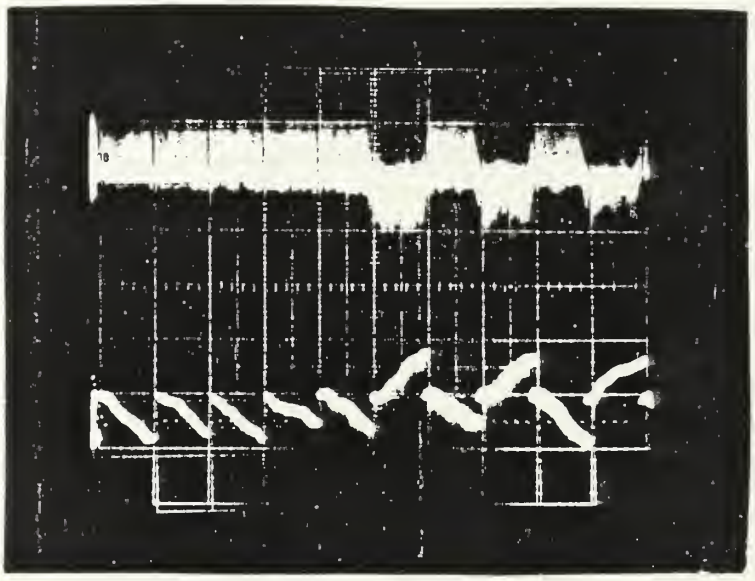


(b)

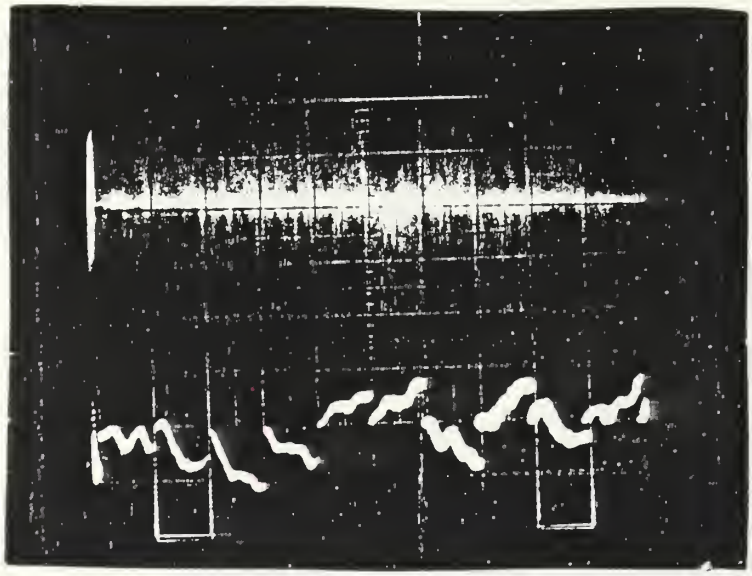
Fig. 3-1. Demodulator Block Diagram (a) and Waveform with Noise (b).

B. THE $\overline{L}$ CIRCUIT WITH NOISE

The integrator recovers the signal from the noise. Fig. 3-2a shows the effect of noise on the demodulated signal at a high SNR. Fig. 3-2b illustrates a demodulator output where the signal is indistinguishable from the noise. The integrator provides a usable output when noise is present.



(a)

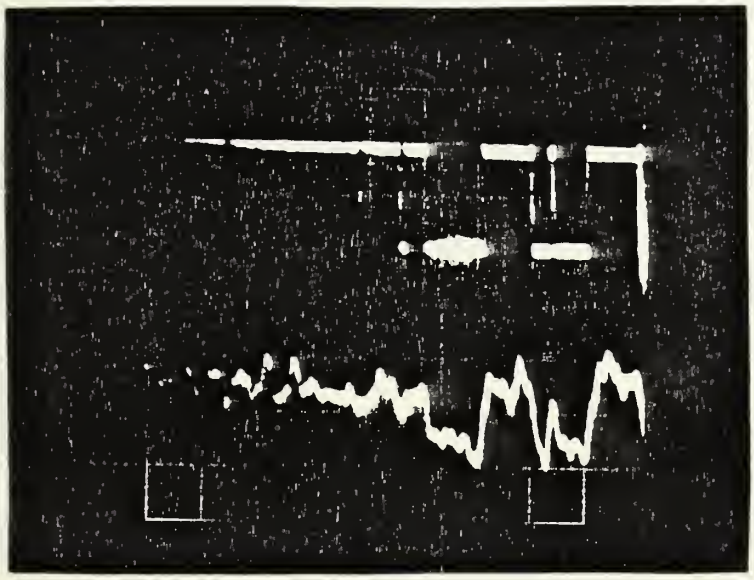


(b)

Fig. 3-2. AVM Output and $\overline{L}$ Integrator Output When Noise Is Present.

C. THE LIMITER (L) WITH NOISE

Figs. 3-3a, b show how noise affects the limiter circuit. The limiter goes to $\pm$4.5 volts when the RC filter output crosses zero volt threshold. Fig. 3-3b shows how the integrator ramps in a piece-wise linear manner.

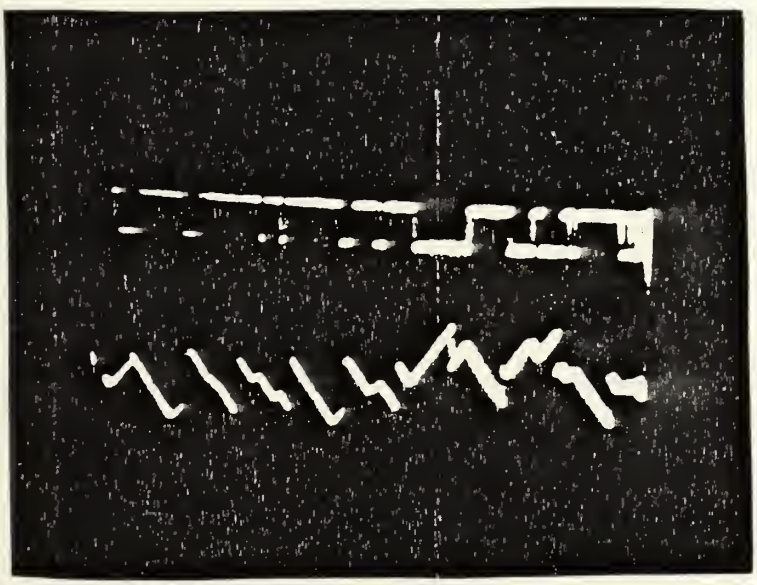


SNR=4.70dB
horz:1msec/div
vert:5v/div

L limiter output

RC filter output

(a)



SNR=2.49dB
horiz:1msec/div
vert:5v/div

Limiter

L Integrator

(b)

Fig. 3-3. Waveforms of Limiter and RC Filter Outputs (a) and Limiter and L Integrator Output (b) When Noise Is Present.

D. ERROR ORIGIN

Knowing the behavior of the L and $\overline{L}$ post-detection circuits, we can speculate on conditions which cause errors in each. The ideal waveform is shown as Fig. 3-4a for a "1". With a little noise added, a likely waveform is shown as Fig. 3-4b. Both L and $\overline{L}$ circuits detect the bit correctly in this case. In Fig. 3-4c, the net area (positive plus negative area) of the voltage over the bit duration is less than zero. Therefore, the integrator output at the end of the bit interval is less than zero and an error occurs. However, the same voltage waveform is above the zero threshold longer than it is below the zero threshold causing the limiter integrator output to be greater than zero at the end of the bit duration, and no error occurs. Fig. 3-4d is the inverse of that situation, where the duration detector circuit, L, makes the error, but $\overline{L}$ is correct. Finally, Fig. 3-4e shows the least likely situation where both L and $\overline{L}$ detectors are in error.

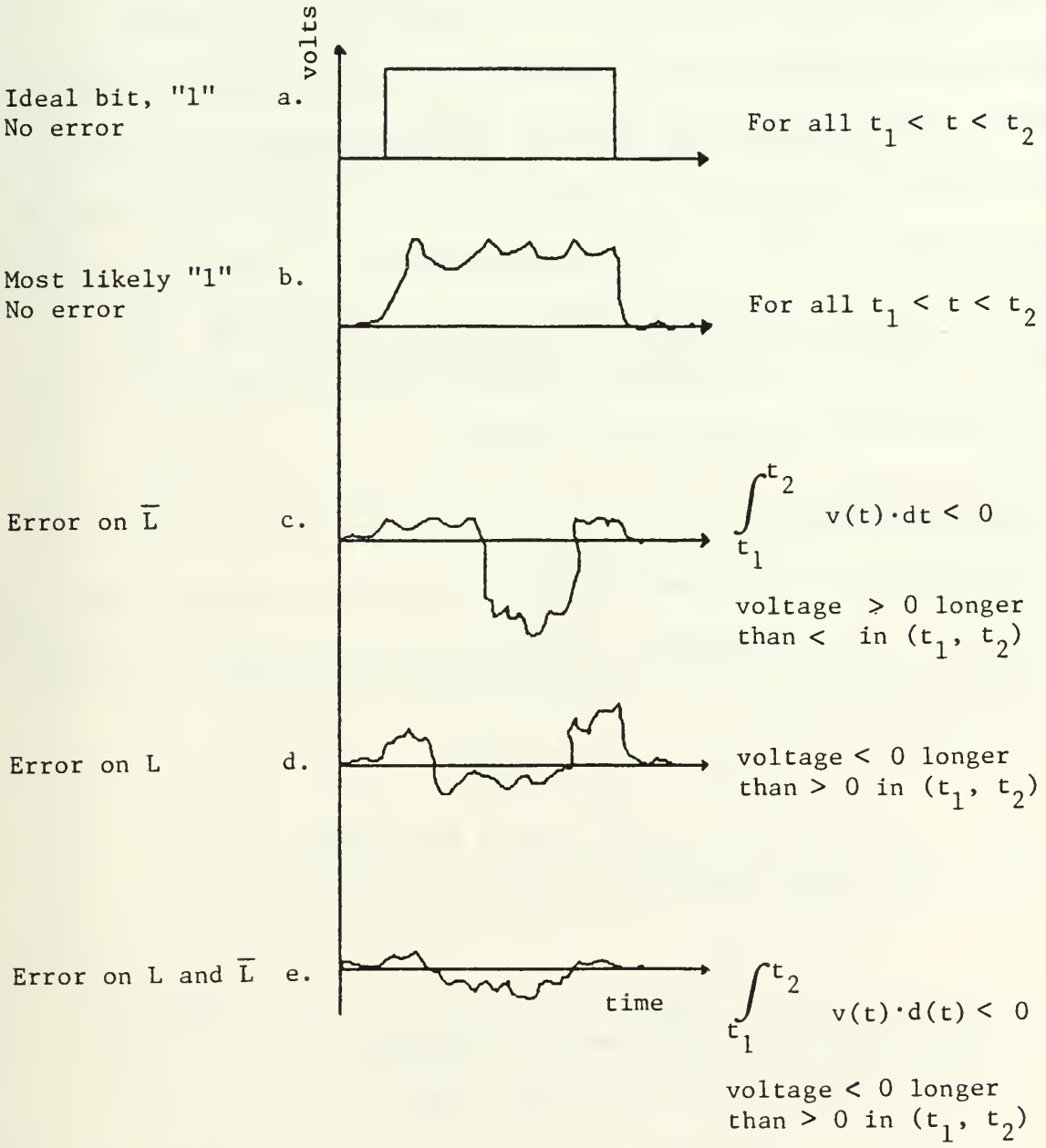


Fig. 3-4. Examples of Voltages Which Do Not (a), (b), and Do (c), (d), (e) Create Errors.

IV. RESULTS

A. GENERAL

The experimental results are taken methodically for a range of signal-to-noise (SNR) ratios. The actual experimental data for one of the data runs is presented in Table I. Table II contains data from larger sample sizes in order to confirm the low probability of error on the curves (10^{-7} range). As explained in Chapter II, Section C, the number of L, $\overline{L}$, and common errors are measured as the noise power is varied. This data is the basis for the performance, correlation, and error type curves presented in this chapter.

B. SYSTEM PERFORMANCE

The performance of the two detectors is measured in terms of the probability of error versus SNR. A data point is calculated as follows:

1. Calculation of SNR

   a. Let V_1=rms voltage of the signal

      V_2=rms voltage of the signal plus noise

      S =signal power

      N =noise power

   b. Then $(V_1^2)/R$ = S where R is the resistive component of the impedance across the true rms voltmeter.

   c. And $(V_2^2)/R$ = signal plus noise (S+N)

   d. (S+N) - S = Noise (N)

   e. SNR (dB) = 10 · (log S/N)

2. Calculation of Probability of Error

TABLE I

EXPERIMENTAL DATA FOR SAMPLE SIZE = 65,536 BITS

V_1 (V rms)	V_2 (V rms)	N (watts)	S/N	10 log S/N dB	Errors $\bar{L}$	Errors L	Errors L and $\bar{L}$
2.830	3.97	7.75	1.03	.14	910	1154	586
2.830	3.93	7.43	1.07	.32	693	919	441
2.830	3.93	7.43	1.07	.32	697	910	456
2.830	3.89	7.12	1.124	.51	514	644	326
2.829	3.86	6.89	1.15	.63	506	684	309
2.829	3.79	6.36	1.25	.99	322	394	197
2.829	3.72	5.83	1.371	1.37	201	273	122
2.829	3.69	5.61	1.425	1.54	1.40	177	71
2.829	3.63	5.18	1.54	1.87	83	133	41
2.829	3.60	4.95	1.61	2.08	78	103	41
2.826	3.57	4.75	1.68	2.24	33	46	14
2.826	3.54	4.54	1.75	2.44	39	50	21
2.826	3.50	4.26	1.87	2.72	22	30	14
2.830	3.47	4.02	1.99	2.99	14	33	11
2.830	3.46	3.95	2.03	3.07	14	19	10
2.830	3.41	3.60	2.22	3.46	6	10	5
2.830	3.38	3.41	2.34	3.71	3	6	3
2.830	3.33	3.09	2.60	4.15	2	0	0
2.830	3.33	3.09	2.60	4.15	1	3	0

TABLE II

EXPERIMENTAL DATA FOR LARGE SAMPLE SIZES

V_1 V rms	V_2 V rms	N (watts)	S/N	10 log S/N dB	Total Bits	Errors $\bar{L}$	Errors L	Errors L AND $\bar{L}$
2.82	3.85	6.84	1.16	.66	4620000	22002	51665	16533
2.78	3.79	6.62	1.16	.67	7920000	34491	59063	23627
2.79	3.44	4.05	1.92	2.83	8100000	973	8103	794
2.95	3.58	4.11	2.11	3.25	3480000	155	312	104
2.87	3.47	3.76	2.19	3.42	3990000	111	238	62
2.87	3.41	3.37	2.44	3.88	4696000	64	144	31
2.85	3.38	3.29	2.47	3.93	38116000	269	1828	103
2.86	3.31	2.76	2.96	4.71	3960000	16	27	6
2.94	3.37	2.71	3.19	5.04	3120000	2	25	2

a. PE($\overline{L}$) = (number of bits in error on $\overline{L}$ detector)/(number of total bits received)

b. PE(L) = (number of bits in error on L detector)/(total number of bits received)

A plot of the performance of the L detector, the $\overline{L}$ detector, and the ideal BPSK detector versus SNR is shown in Fig. 4-1a, b with the data points listed in Table III. The $\overline{L}$ detector appears to perform better than the L detector for each SNR by approximately 0.2 dB. Notice that both the L and $\overline{L}$ curves are three to four decibels better than the typical BPSK PE curve. This is becuase the SNR at the output of the matched filter (integrate and dump) normally expressed as E_b/N_o is twice the SNR at the input to the modulator ($E_b/N_o = (SNR)_{IN} \cdot (BW/f) = (SNR)_{IN} \cdot 2$) [Ref. 1: p. 158].

C. CORRELATION

In this experiment, correlation is defined as the number of bits in error which are common to both the L and $\overline{L}$ detectors divided by the average number of errors made by the L and $\overline{L}$ detectors. For example:

Let N_L = number of errors for L detector

$N_{\overline{L}}$ = number of errors for $\overline{L}$ detector

N_C = number of errors in common

Then correlation $C = N_C/((N_L + N_{\overline{L}})/2)$

The error and correlation data is presented in Table IV. A plot of correlation versus SNR (in dB) in Fig. 4-2 shows a somewhat linear change in correlation with SNR. As may be expected at a low SNR the high noise power causes both the L and $\overline{L}$ detectors to make an error on

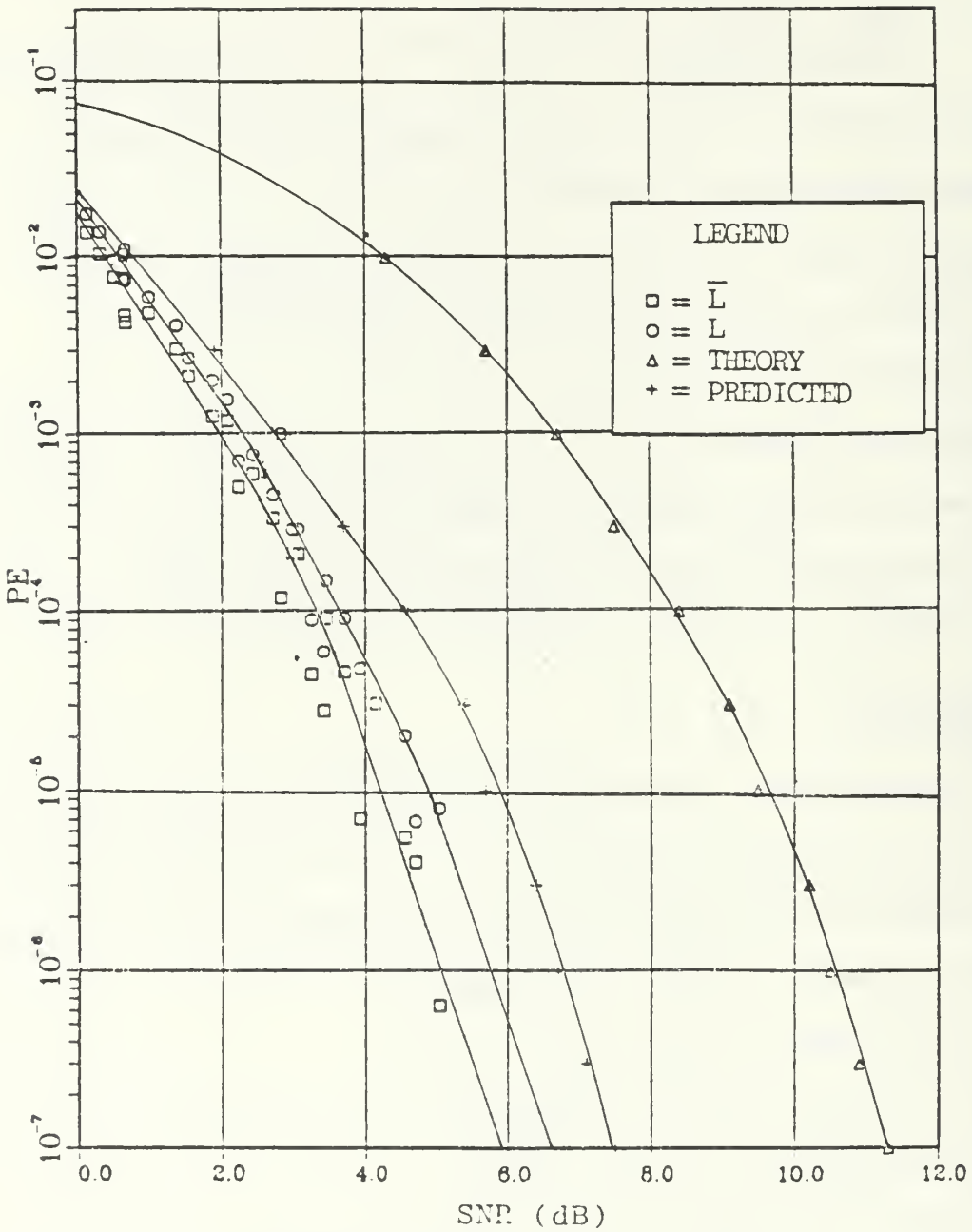


Fig. 4-1a. Probability of Error vs SNR for $\bar{L}$ and L Circuits, Ideal BPSK, and Predicted Experimental Results Based on BW = 2.4 kHz.

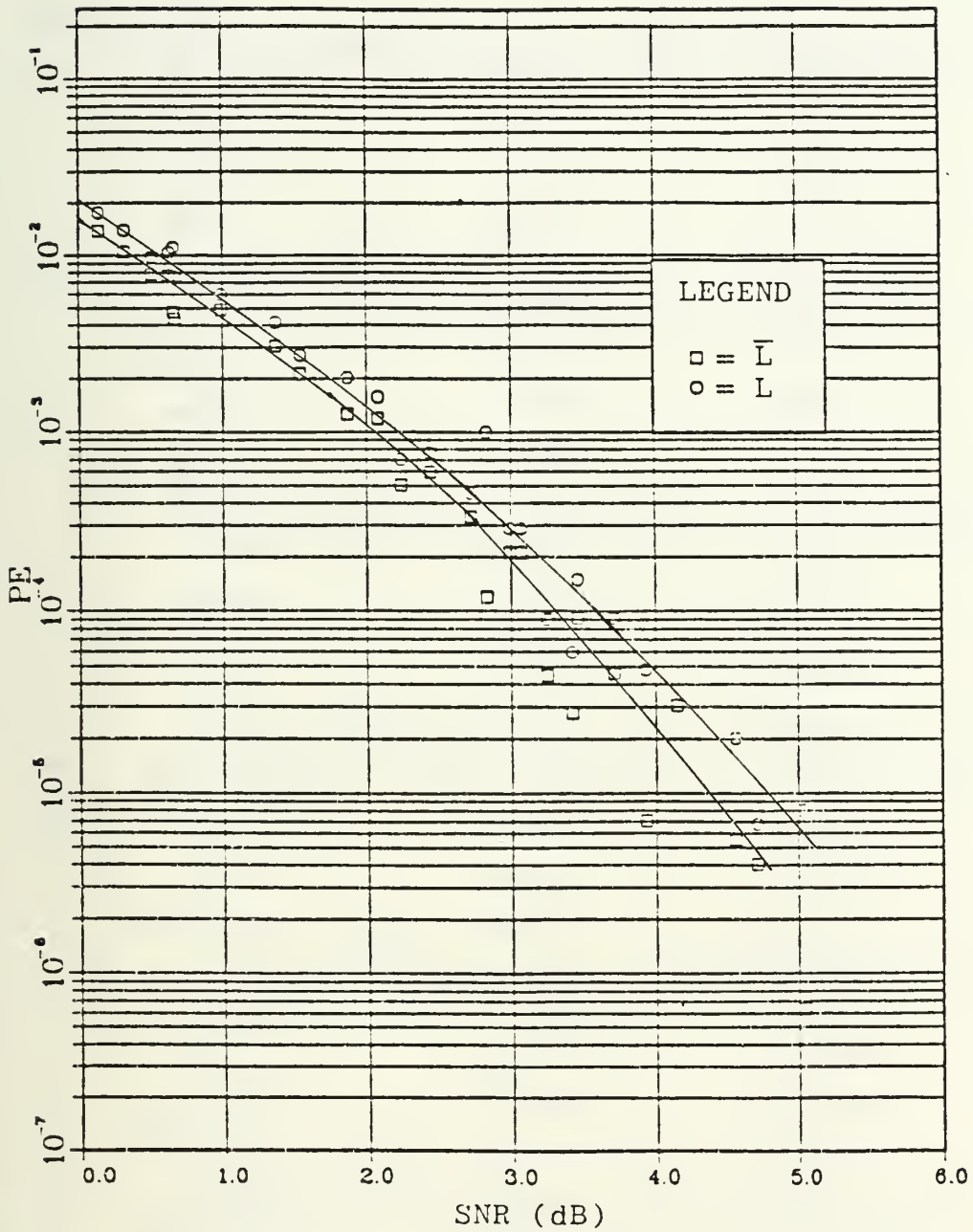


Fig. 4-1b. Probability of Error vs SNR for L and $\bar{L}$ Circuits (expanded).

TABLE III
PE v SNR DATA POINTS

SNR(dB)	$\bar{L}$ PE	L PE	TOTAL BITS TRANSMITTED
0.14	.0139	.0176	65536
0.32	.0105	.0140	65536
0.32	.0106	.0139	65536
0.51	.00784	.00982	65536
0.63	.00772	.0104	65536
0.66	.00476	.0111	4620000
0.67	.00435	.00745	7920000
0.99	.00491	.00601	65536
1.37	.00306	.00416	65536
1.54	.00213	.00270	65536
1.87	.00126	.00202	65536
2.08	.00119	.00157	65536
2.24	.000503	.000702	65536
2.44	.000595	.00763	65536
2.72	.000335	.000457	65536
2.83	.00012	.001	8100000
2.99	.000213	.000503	65536
3.07	.000213	.000289	65536
3.25	.0000445	.0000896	3480000
3.42	.0000278	.0000596	3990000
3.46	.000091	.00015	65636
3.71	.0000457	.0000915	65536
3.93	.00000705	.0000479	38116000
4.15	.0000152	.0000457	65535
4.56	.00000555	.0000201	1440000
4.71	.00000404	.00000681	3960000
5.04	.000000641	.00000801	3120000

TABLE IV
ERROR TYPE AND CORRELATION DATA

S/N	$N_{\overline{L}}$	N_L	N_C	D $\overline{L}$ UNIQUE	E L UNIQUE	C CORRELATION
0.14	910	1154	586	324	568	.57
0.32	693	919	441	252	478	.55
0.51	514	644	326	188	318	.56
0.63	506	684	309	197	375	.52
0.66	22.002	51665	16553	6469	35132	.64*
0.67	34.491	59063	23627	10764	35436	.51*
0.99	322	394	197	125	197	.55
1.37	201	273	122	79	151	.51
1.54	140	177	71	69	106	.45
1.87	83	133	41	42	92	.38
2.08	78	103	41	37	62	.45
2.24	33	46	14	19	32	.35
2.44	39	50	21	18	29	.47
2.72	22	30	14	8	16	.54
2.83	973	8103	794	179	7309	.17*
2.99	14	33	11	3	22	.47
3.07	14	19	10	4	9	.61
3.25	155	312	104	51	208	.45*
3.42	111	238	62	49	176	.36*
3.46	7	10	5	1	5	.625
3.71	3	6	3	0	3	.33
3.88	64	144	31	33	113	.30*
3.93	269	1828	103	166	1725	.10*
4.15	2	0	0	2	0	0
4.15	1	3	0	1	3	0
4.56	8	29	2	6	27	.11*
4.71	16	27	6	10	21	.28*
5.04	2	25	2	0	23	.15*

* These data are from large sample sizes.

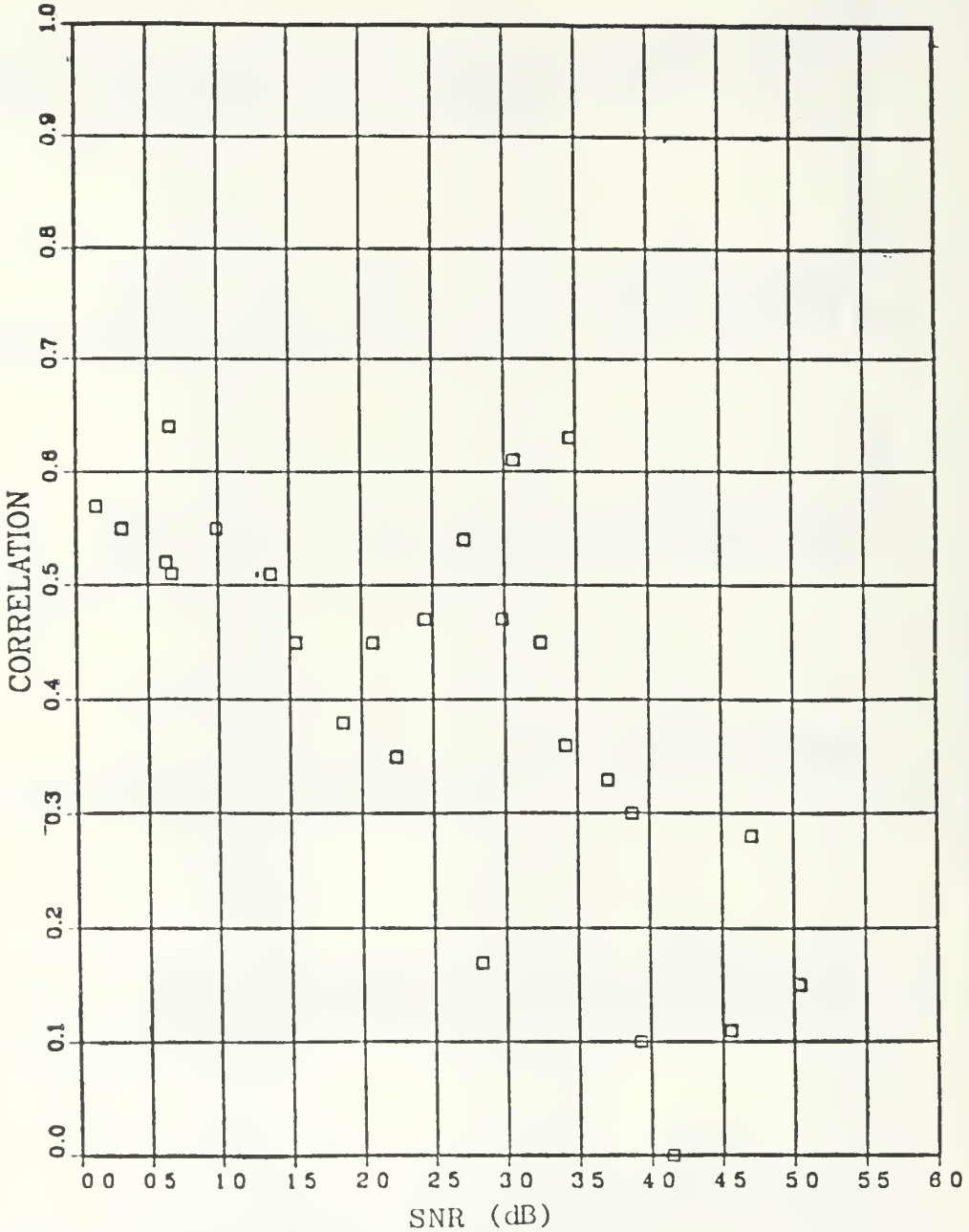
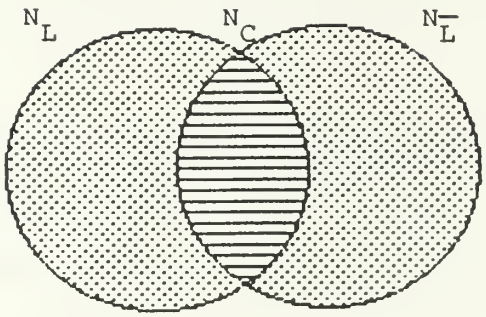


Fig. 4-2 Correlation vs SNR (dB)

the same bit more often and the correlation is approximately 0.6. At higher SNR ratios the errors are less correlated, that is the L and $\overline{L}$ detectors will less frequently make an error on the same bit.

D. ERROR TYPES

A description of the three types of errors was presented in Section D of Chapter III. There are three types of errors. One type of error is unique to the L detector. A second type of error occurs only on the $\overline{L}$ detector, while the third type is an error made in common by the two detectors. The specific data of error types, SNR, and correlation is presented in Table IV. A diagram illustrating the classification of errors into these sets is presented in Fig. 4-3. The overlap region, N_C, is the set of errors in common to the L and $\overline{L}$ circuits, where the random voltage for that "1" bit spends more time below the threshold than above it, while the integrator output at the sample time is negative rather than positive. A plot of the number of common errors versus SNR is shown in Fig. 4-4. The $\overline{L}$ circuit unique errors are illustrated as set E in the Venn diagram (Fig. 4-3) and plotted in Fig. 4-5 as a function of SNR. The limiter circuit unique errors, are shown as set D and plotted versus SNR is Fig. 4-6. Fig. 4-7 compares these three error types on the same graph. It establishes that these three error types occur with different probabilities. The L error occurs the most often over each SNR. The $\overline{L}$ unique error occurs the least often and the common error occurs in the range somewhere between the other two errors.



N_C = NUMBER of ERRORS MADE by BOTH L and $\bar{L}$ CIRCUITS on the SAME BIT

N_L = NUMBER of ERRORS from L CIRCUIT

$N_{\bar{L}}$ = NUMBER of ERRORS from $\bar{L}$ CIRCUIT

$D = N_{\bar{L}} - N_C$ = NUMBER of ERRORS MADE by $\bar{L}$ CIRCUIT and NOT by L CIRCUIT

$E = N_L - N_C$ = NUMBER of ERRORS MADE by L CIRCUIT and NOT by $\bar{L}$ CIRCUIT

Fig. 4-3. Classification of Error Types.

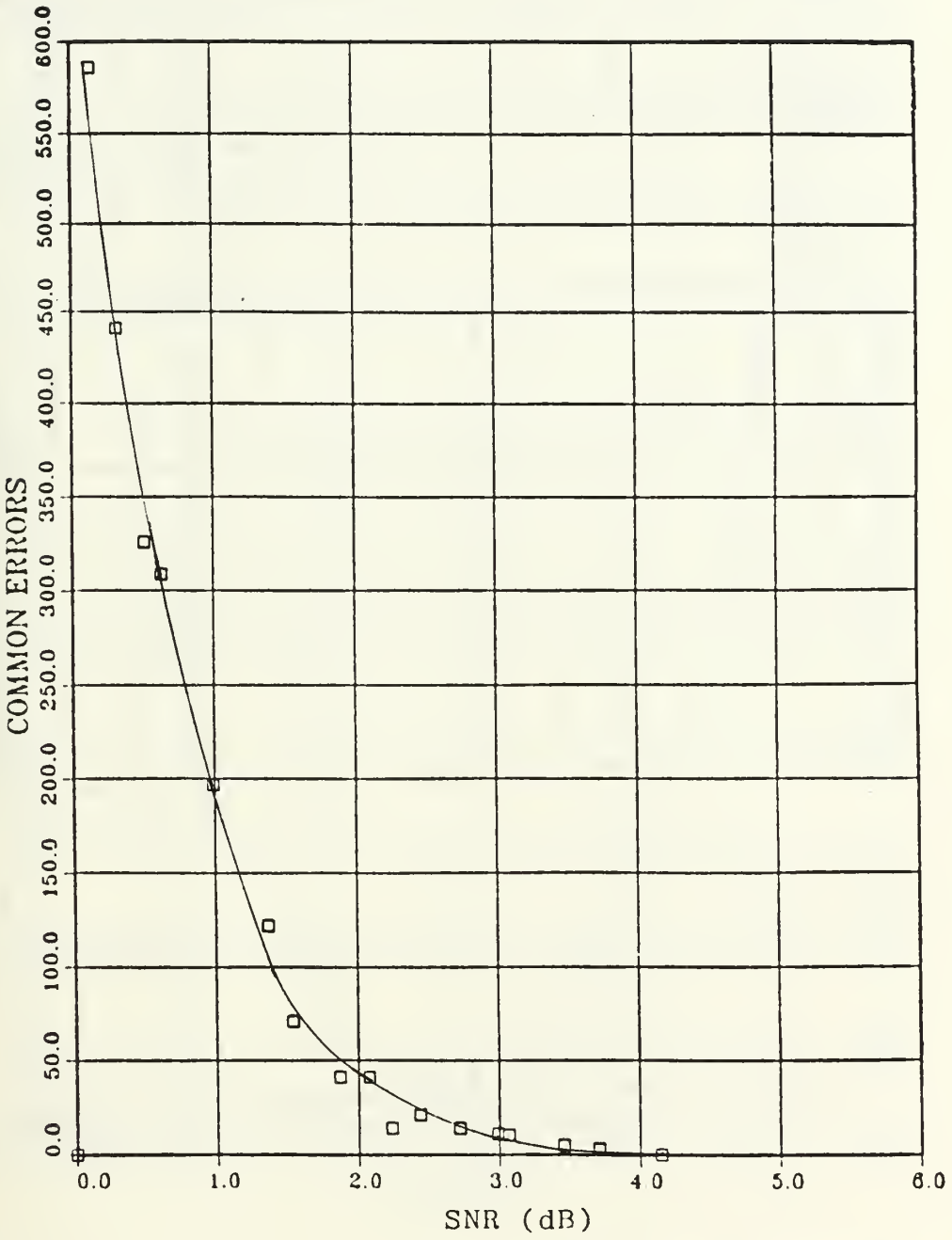


Fig. 4-4. Common Errors vs SNR (dB).

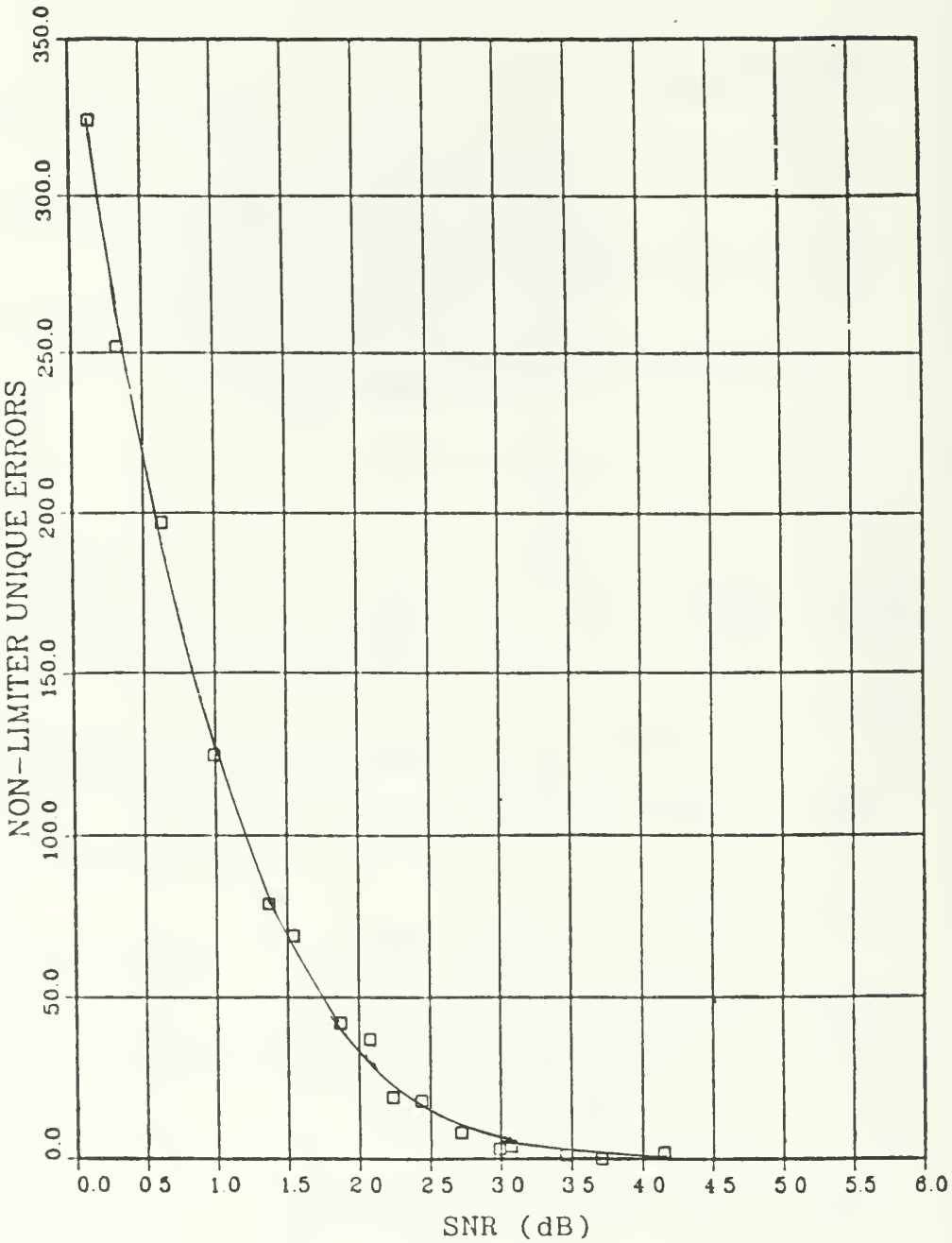


Fig. 4-5. Non-Limiter Unique Errors vs SNR (dB).

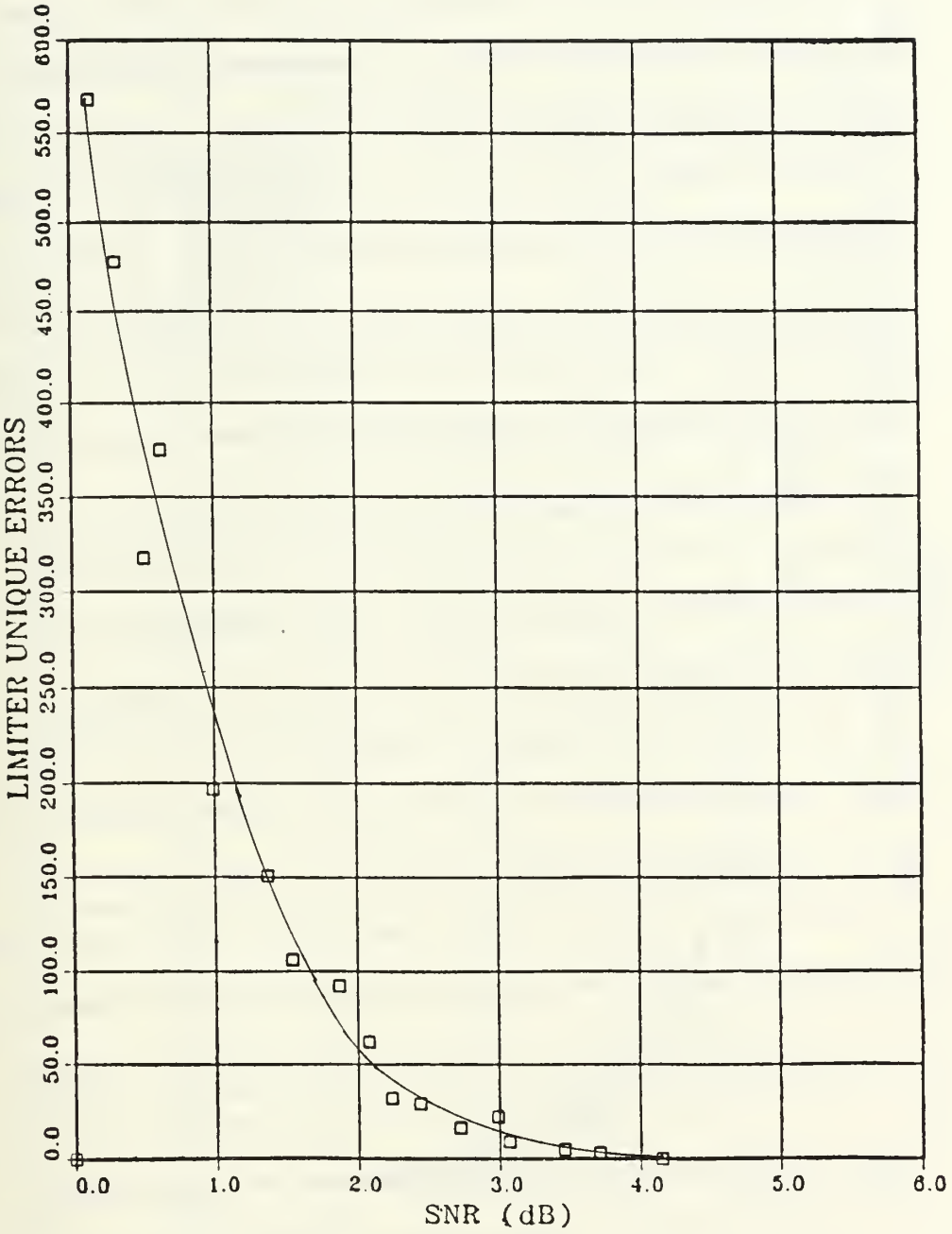


Fig. 4-6. Limiter Unique Errors vs SNR (dB).

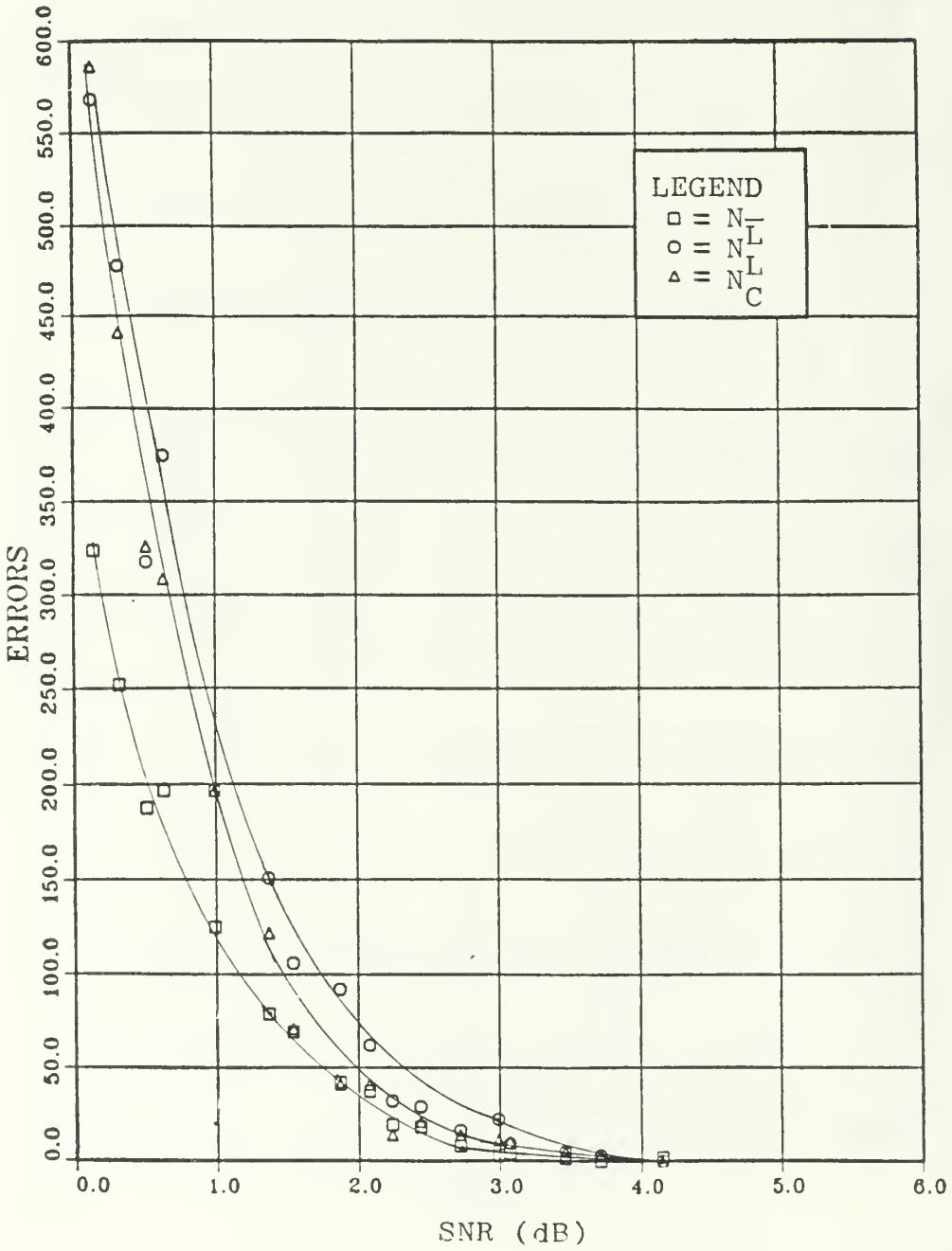


Fig. 4-7. Limiter Unique, Non-Limiter Unique, and Common Errors vs SNR(dB).

E. VERIFICATION OF THE DATA

The experimental results are verified by several techniques. First, five data sets in general agreement were taken. Second, the circuitry after the integrate and dump (the sample and hold, error detection, and counter circuitry) were switched between the L and $\overline{L}$ circuits. Similar error counts were obtained before and after the switch for the same SNR ratio. This technique verified that the circuitry for both channels after the integrate and dump was working correctly. A third method for verifying the data which also gives insight into the results is to take probability density functions (PDF). A Spectral Dynamics 360 Digital Signal Processor is used to produce Figs. 4-8 through 4-14. Fig. 4-8a and b shows the output of the $\overline{L}$ integrator without noise and with noise added for a random binary data input. Fig. 4-8a shows a uniform distribution of the of the $\overline{L}$ integrater without noise and with noise added for a random binary data input. Fig. 4-8a shows a uniform distribution of the integrator except for a small peak around 0 volts. When noise is added the distribution takes on a Gaussian shape (b). Figs. 4-8c and 4-8d show a somewhat different distribution for the limiter circuit. Fig. 4-8c shows two uniform levels for the L circuit without noise. This second level reflects the transition time of the RC filter output between positive and negative levels. Fig. 4-8d shows smoothing of the distribution when noise is added. The symmetry and uniformity in these two distributions is an indication that these two circuits are working properly. Figs. 4-9 and 4-10 show the PDFs of the sample and hold output with a random binary data input. In Fig. 4-9a, all

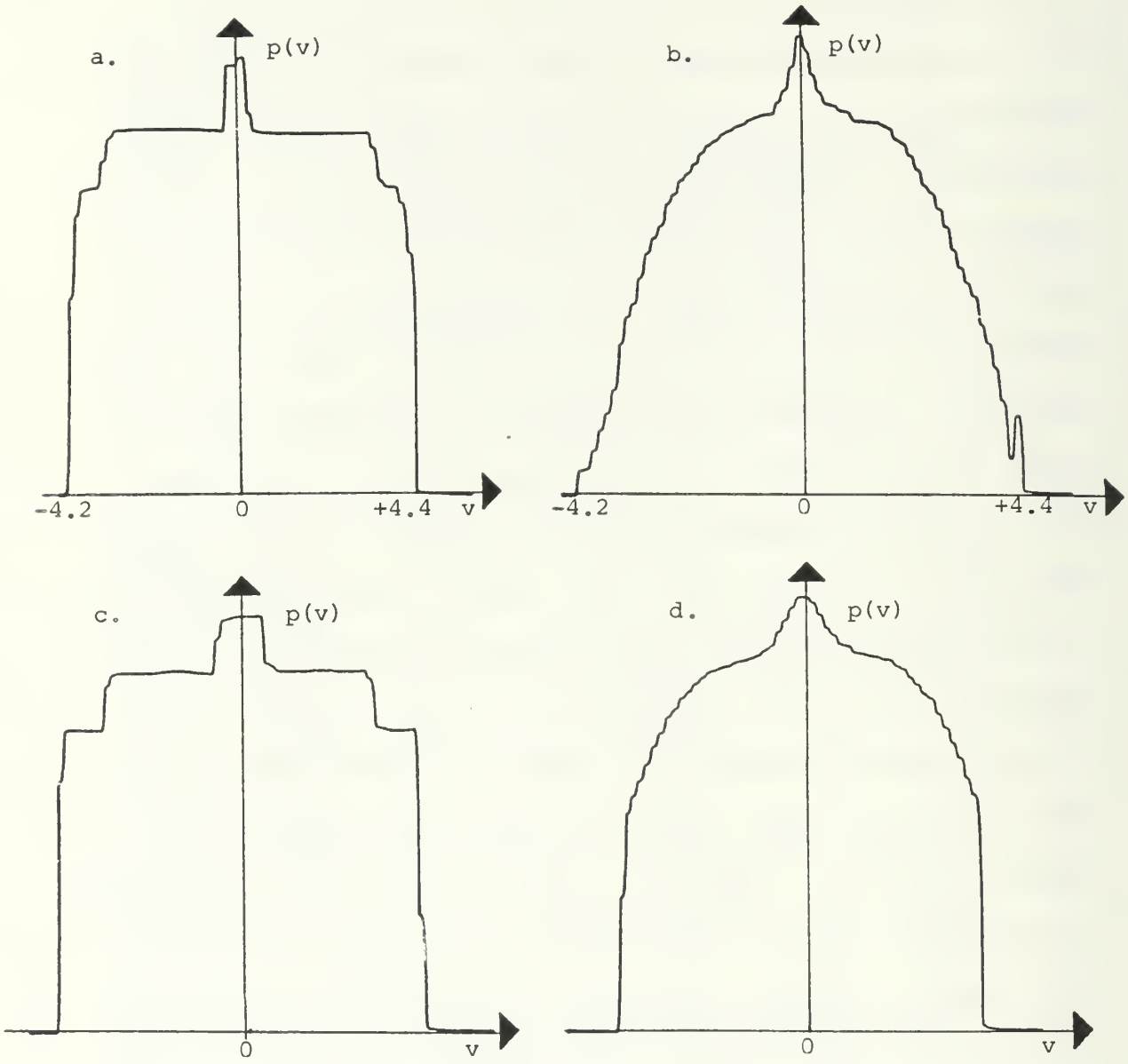


Fig. 4-8. a. PDF of $\overline{L}$ Integrator Output without Noise.
b. PDF of $\overline{L}$ Integrator Output when SNR = 1.15 dB.
c. PDF of L Integrator Output without Noise.
d. PDF of L Integrator Output when SNR = 1.15 dB.

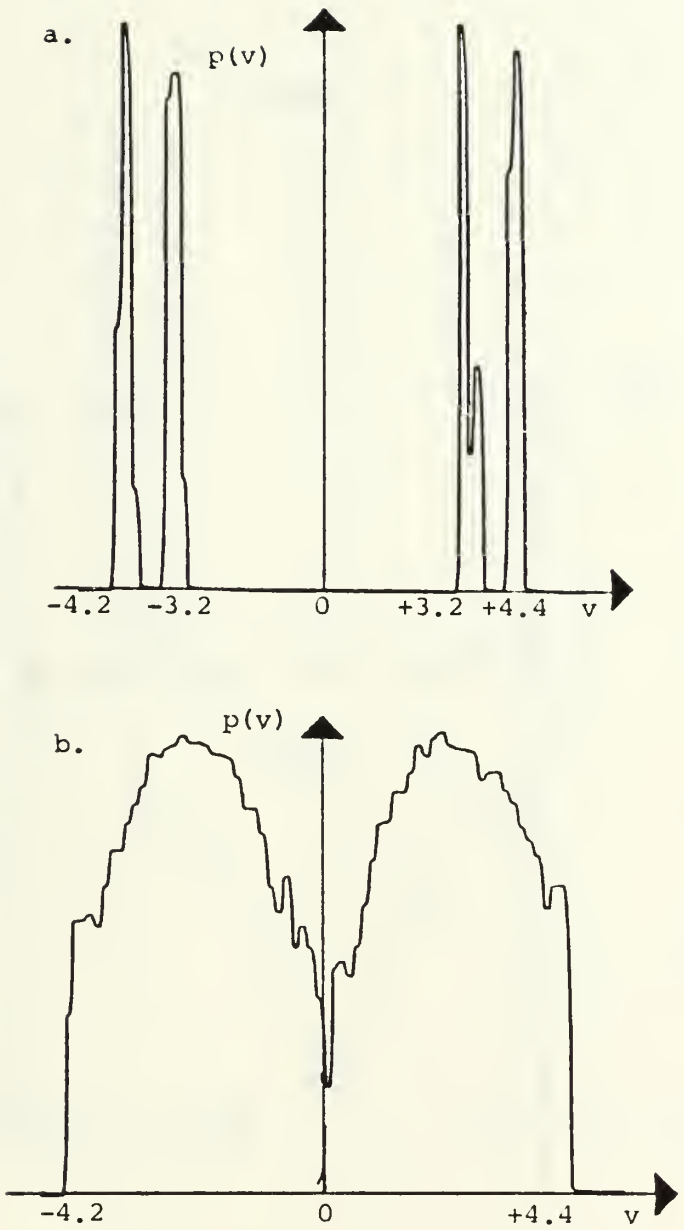


Fig. 4-9. a. PDF of $\overline{L}$ Sample and Hold Output without Noise.
b. PDF of $\overline{L}$ Sample and Hold Output when SNR = 1.15 dB.

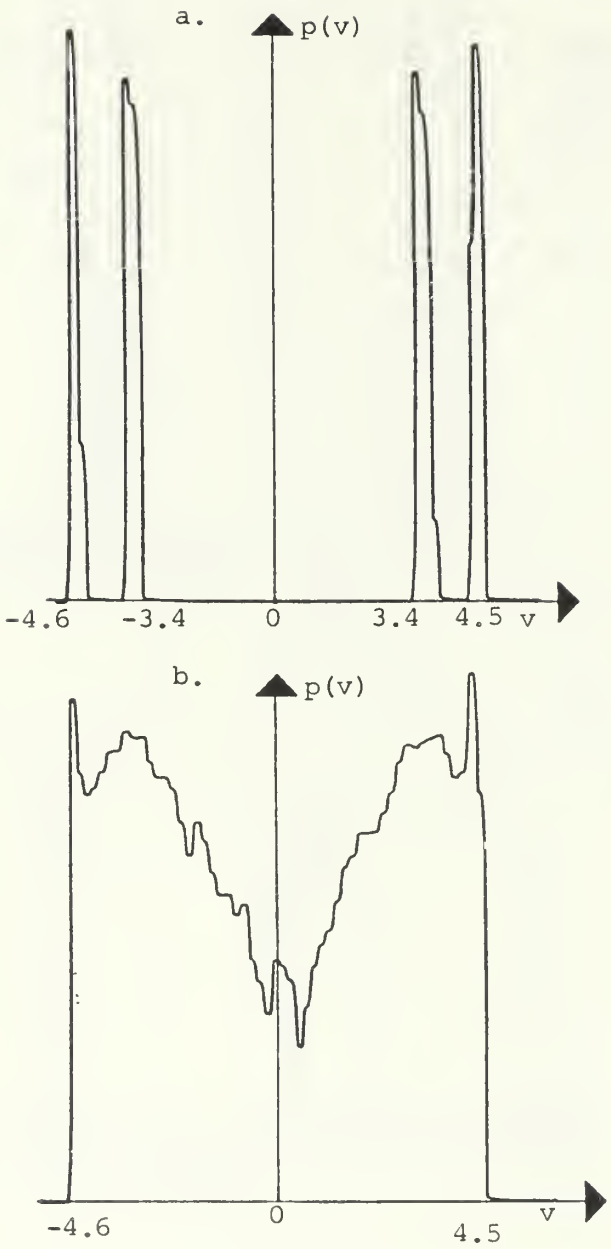


Fig. 4-10. a. PDF of L Sample and Hold Output without Noise.
b. PDF 1f L Sample and Hold Output when SNR = 1.15 dB.

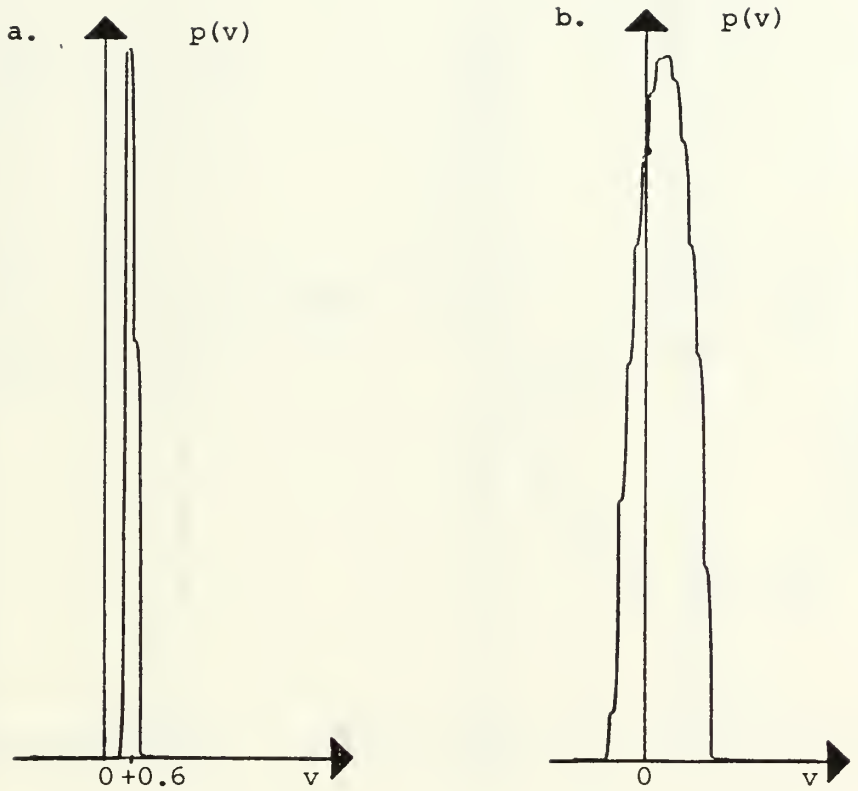


Fig. 4-11. a. PDF of RC Filter Output on L Circuit without Noise with All 1's Data.
b. PDF of RC Filter Output on L Circuit when SNR = 1.15 dB with All 1's Data.

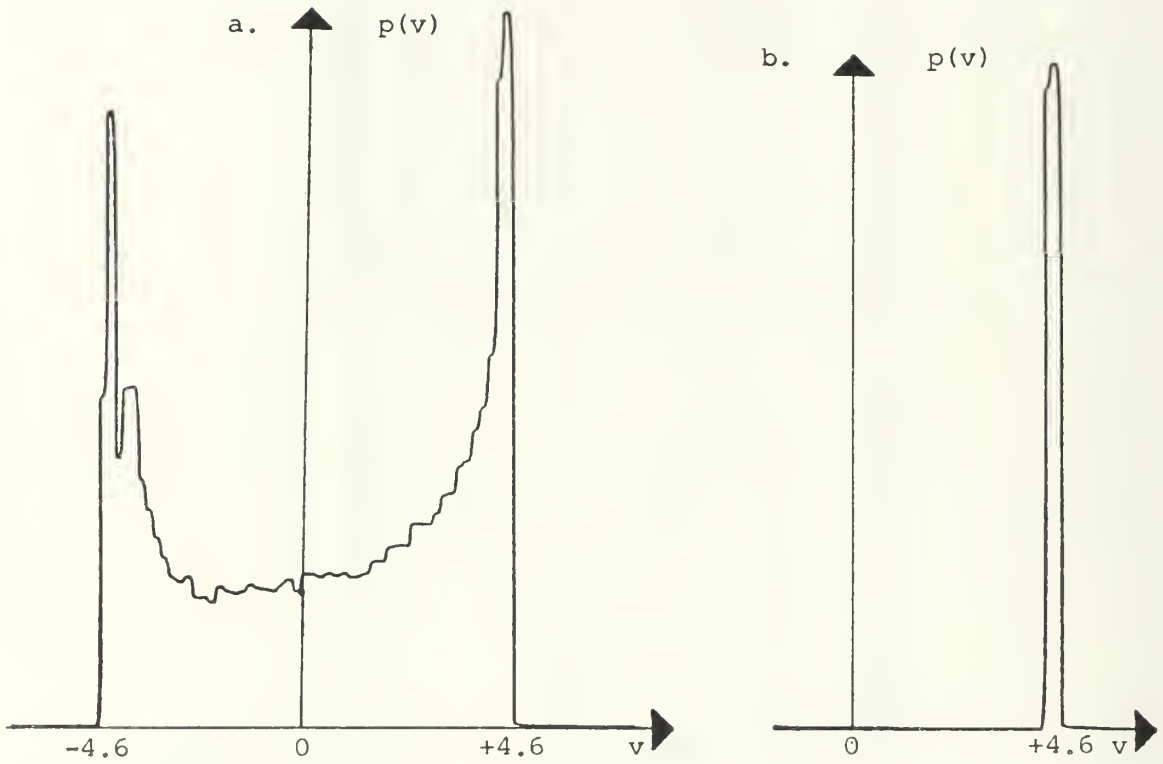


Fig. 4-12. a. PDF of Limiter Output when SNR = 1.15 dB with All 1's Data.
b. PDF of Limiter Output without Noise and with All 1's Data.

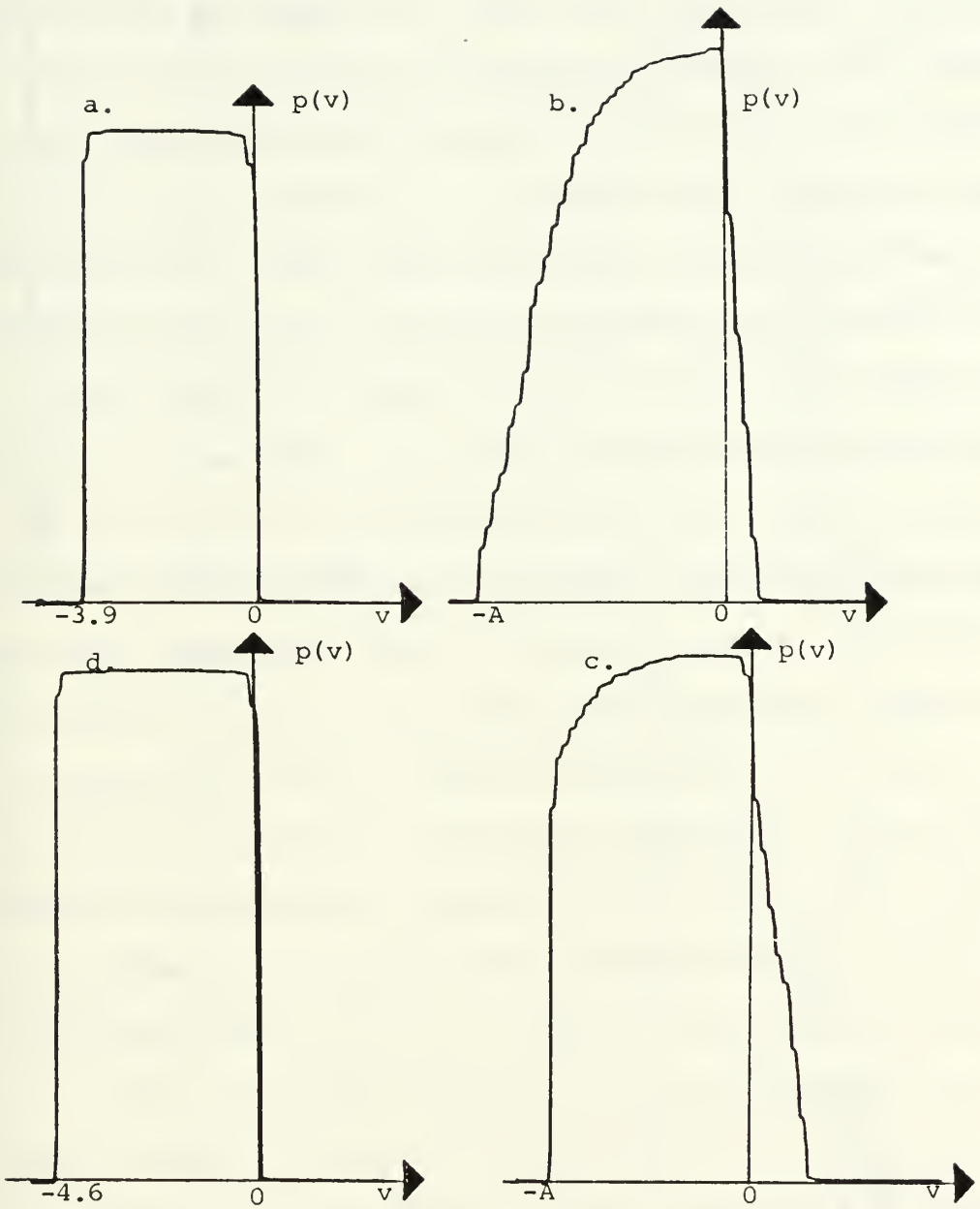


Fig. 4-13. a. PDF of $\overline{L}$ Integrator Output without Noise with All 1's Data.
b. PDF of $\overline{L}$ Integrator Output when SNR = 1.15 dB with All 1's Data.
c. PDF of L Integrator Output without Noise with All 1's Data.
d. PDF of L Integrator Output when SNR = 1.15 dB with All 1's Data.

samples are transmitted with no noise and are at +A or -A volts (no errors). The two spikes at each level occur because of the differing integrator outputs between consecutive 1's (or 0's) and a 0-1 (1-0) transition. Fig. 4-9b shows two Gaussian-like distributions, again symmetric about the 0 volt threshold. Fig. 4-10a, b shows the PDFs of the L sample and hold output for random binary data. Note the somewhat linear decrease in the distribution instead of the rounded Gaussian PDF seen in Fig. 4-9b. In Fig. 4-11a, the output of RC filter is a constant positive DC voltage when there is no noise and all 1's data. When noise is added, the output is Gaussian with a positive DC mean value, shown in Fig. 4-11b. Notice how the noise increases the width of the distribution which is directly related to the noise power added to the signal. The PDFs of the limiter output with all 1's data are shown in Fig. 4-12. When noise is added, the limiter PDF shows two spikes indicating the positive and negative levels of the limiter. The continuous region indicates the switching time between the two levels (Fig. 4-12a). Without noise the limiter remains at a constant 4.6v volts (Fig. 4-12b) for all 1's input. Fig. 4-13 presents the PDFs of the L and $\overline{L}$ integrator with all 1's data. Observe that the L integrator has more area to the right of 0 volts (d) than does the $\overline{L}$ integrator (b) indicating a larger probability of error. Without noise (Figs. 4-13a, d), uniform distributions between a negative voltage and 0 volts occur as expected. The PDFs of the sample and hold outputs for all 1's data are shown in Fig. 4-14. In Fig. 4-14b the samples are Gaussian distributed about some mean value which has shifted to a more positive value. The samples to the right of the zero volt threshold

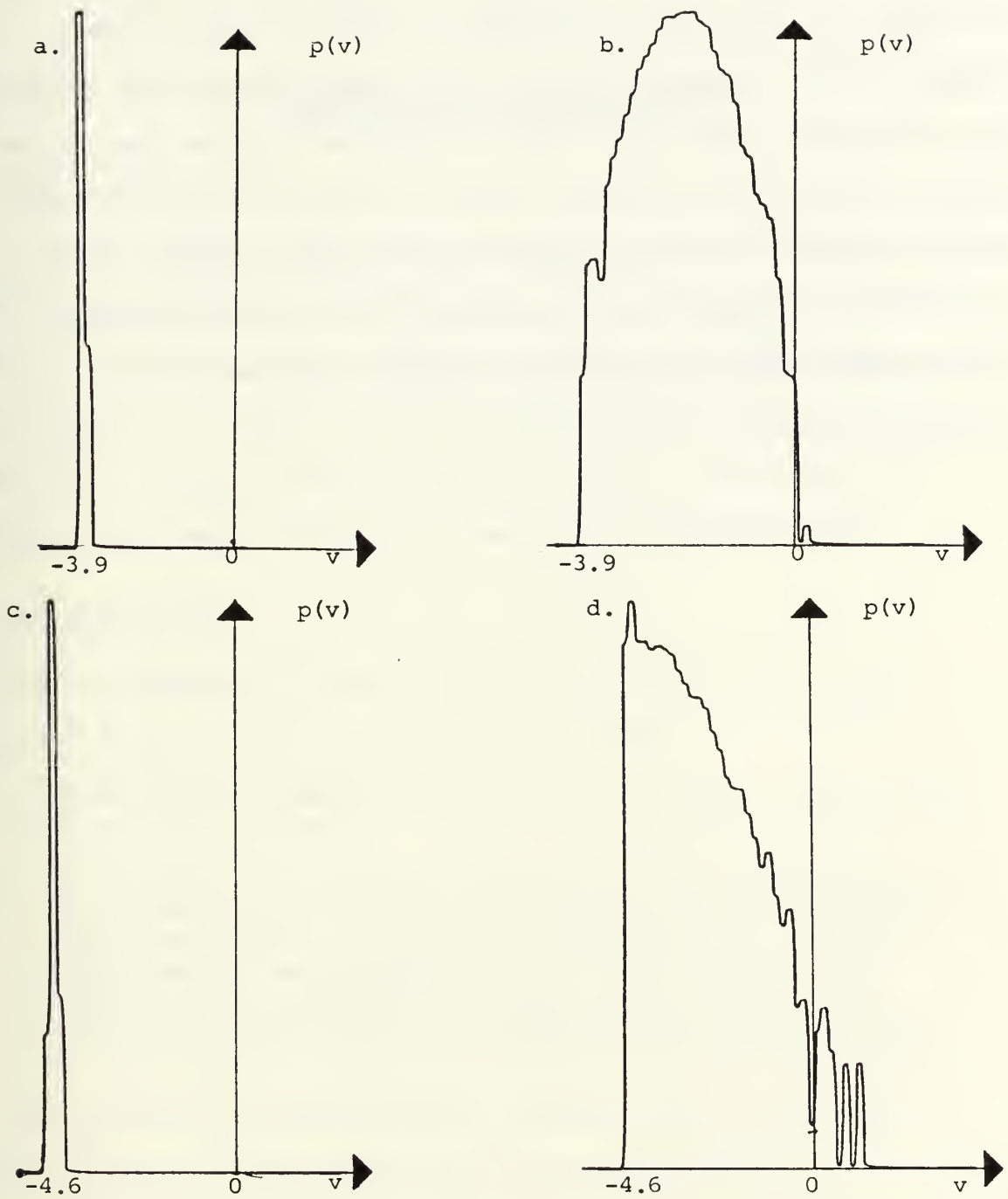


Fig. 4-14. a. PDF of $\overline{L}$ Sample and Hold Output without Noise with All 1's Data.
b. PDF of $\overline{L}$ Sample and Hold Output when SNR = 1.15 dB with All 1's Data.
c. PDF of L Sample and Hold Output without Noise with All 1's Data.
d. PDF of L Sample and Hold Output when SNR = 1.15 dB with All 1's Data.

are errors. In Fig. 4-14d, the number of samples in the L circuit display a steady decrease from -4.6 volts across the zero volt threshold into the positive volt range. The L circuit has a greater area to the right of the zero volt threshold than the $\overline{L}$ circuit at SNR = 1.15 dB. This is confirmed by the experimental data in Fig. 1-1 (BPSK PE versus SNR). All these results (probability density functions and experimental techniques) verify that the data taken during the experiment is valid.

V. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

A conclusion that can be drawn from the data is that the $\overline{L}$ circuit performs approximately 0.2 dB better than the L circuit over all SNR ratios. This result is consistent for each run of the experiment and provides some insight into how each type of error is made in a BPSK system. However, better low pass filtering to reduce the high frequency noise before limiting may change the performance curves.

B. RECOMMENDATIONS

More information is needed to improve the decision made on each bit. The present decision process is as follows:

1. If the error is common between the $\overline{L}$ and L circuits then the bit is accepted as an error.

2. If the error is an $\overline{L}$ unique error and not an L unique error, or vice versa, there is no way to know if a 1 or a 0 is sent for a random binary input. Therefore a decision for the $\overline{L}$ circuit guarantees the least amount of errors according to the mathematically derived BPSK PE curves. It is obvious that without more information, the correlation data between the L and the $\overline{L}$ circuitry cannot be utilized in the decision process.

The addition of a third detection circuit to the L and $\overline{L}$ circuits allows a majority logic decision device to be implemented. This voting technique decides a 1 if two or more of the three circuits decided a 1. Fig. 5-1 illustrates the seven error regions for this concept. A majority logic diagram and truth table are presented in Fig. 5-2. Experimentation will determine the performance of this system.

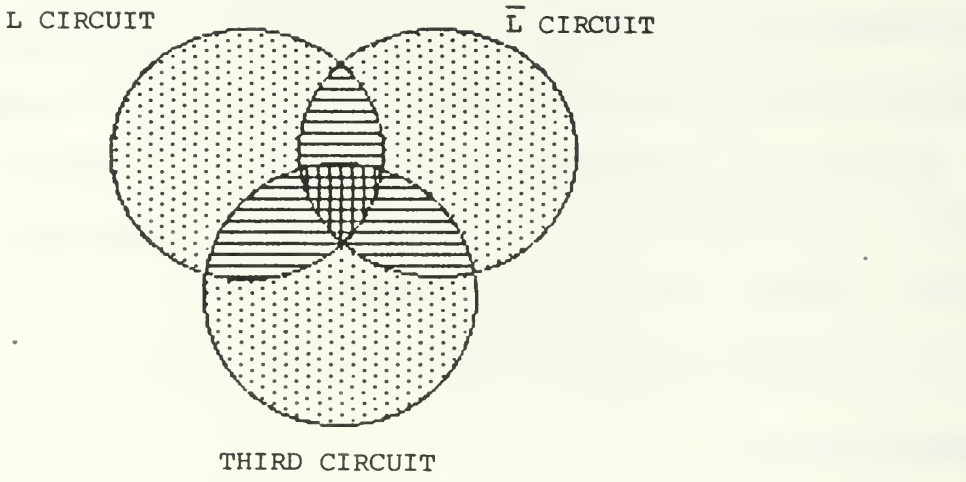
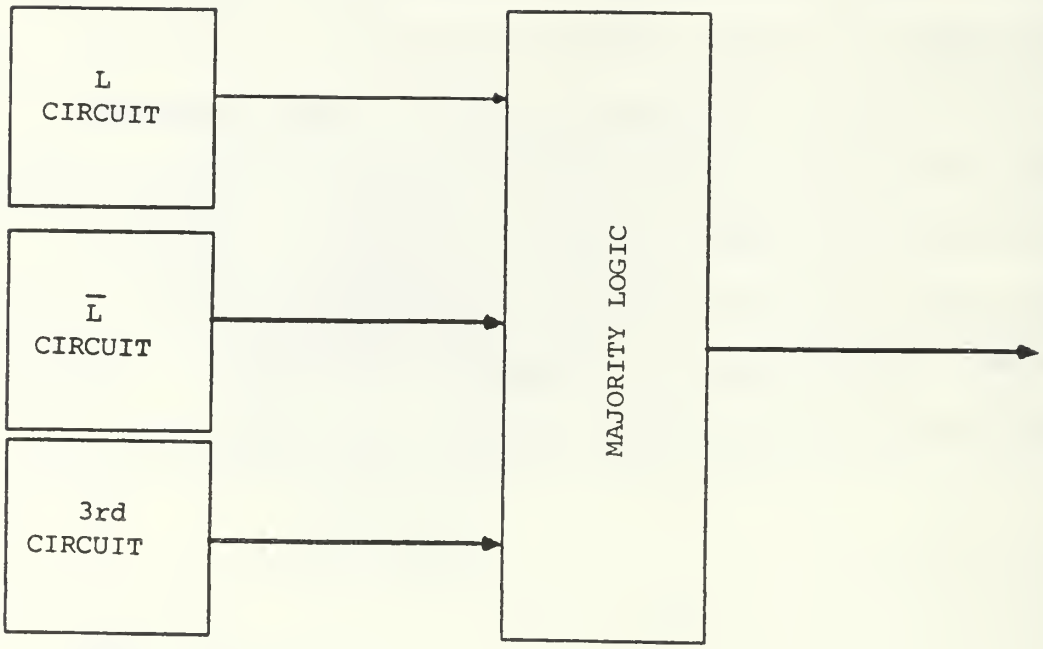


Fig. 5-1. Error Regions for Three BPSK Receivers.

No specific design for the third circuit is obvious. The signal plus noise voltage can be described in terms of amplitude, phase, and frequency. These three parameters are known for the signal and are random variable for noise. Coherent demodulation uses the known phase and frequency of the signal to align the local oscillator. Perhaps a third detection technique can be designed by demodulating with the local oscillator offset in phase from the signal phase. This provides results different from that of the L and $\overline{L}$ circuitry allowing for further correlation and classification of error types. The effect of various values of phase offset requires further experimentation.



Input			Output =	
L	$\overline{L}$	3rd	L + $\overline{L}$ + 3rd	Decision
0	0	0	0	no error
0	0	1	0	3rd circuit unique error
0	1	0	0	$\overline{L}$ circuit unique error**
0	1	1	1	$\overline{L}$ and 3rd common error
1	0	0	0	L circuit unique error
1	0	1	1	L and 3rd common error
1	1	0	1	L and $\overline{L}$ common error
1	1	1	1	L, $\overline{L}$, and 3rd common error

** Note: A 1 may be decided in this case (and not use majority logic), because it may prove that when only the $\overline{L}$ circuit is in error, it will be the best decision. This concept can only be verified through experiment.

Fig. 5-2. Majority Logic Diagram and Truth Table.

APPENDIX
CIRCUIT DIAGRAMS

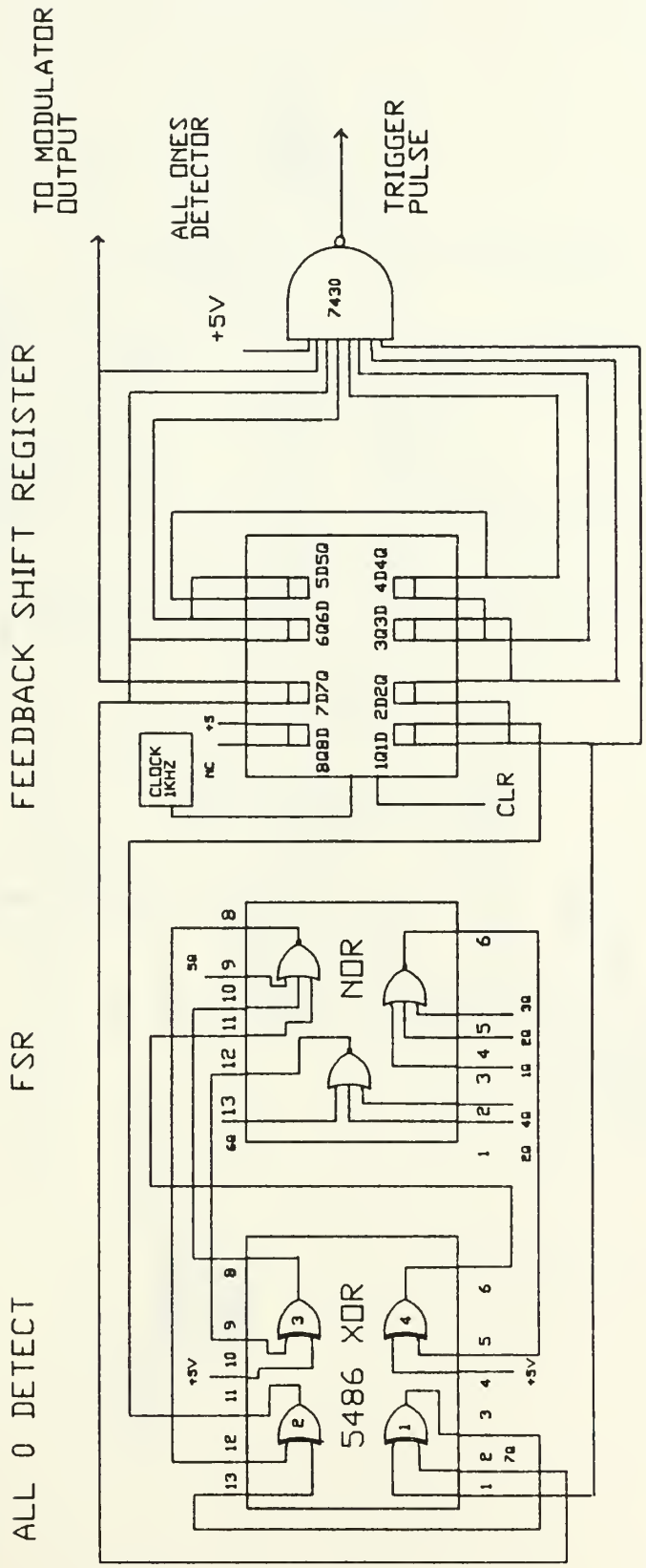


Fig. A-1. Data Source Circuit.

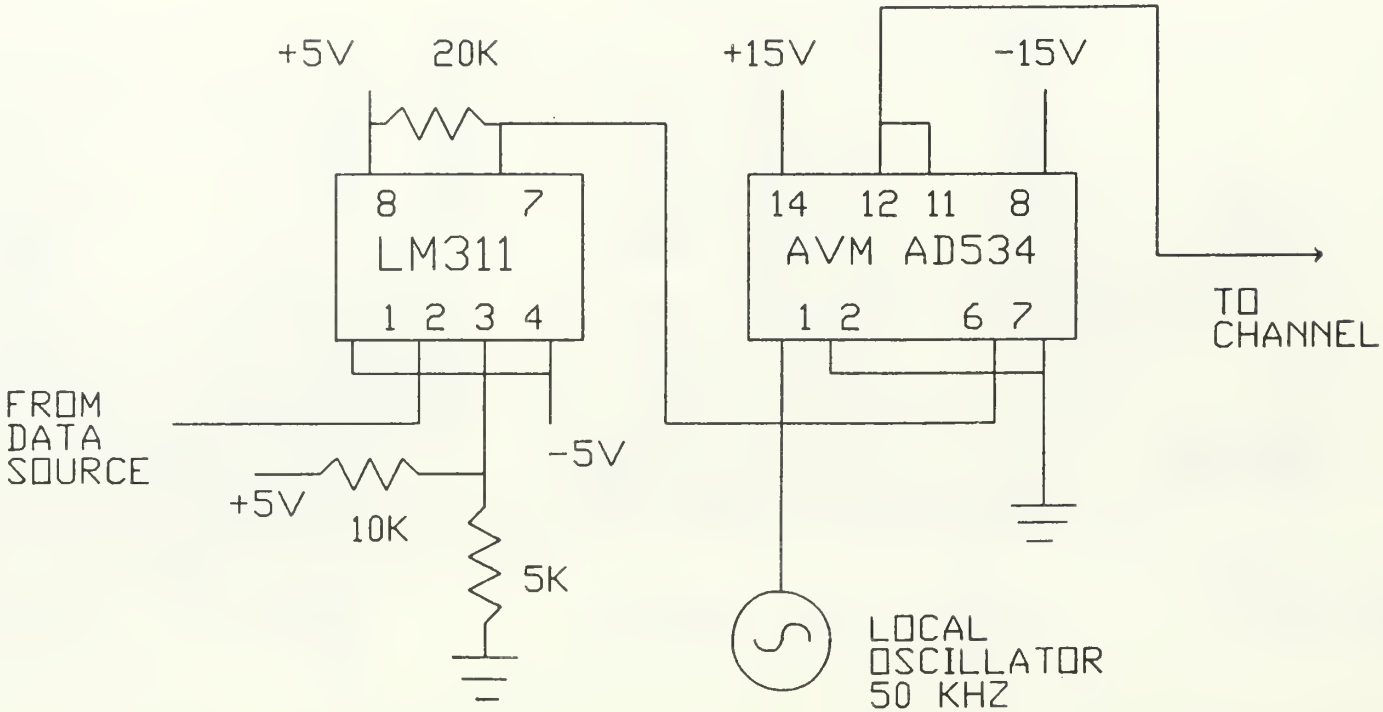


Fig. A-2. Modulator Circuit.

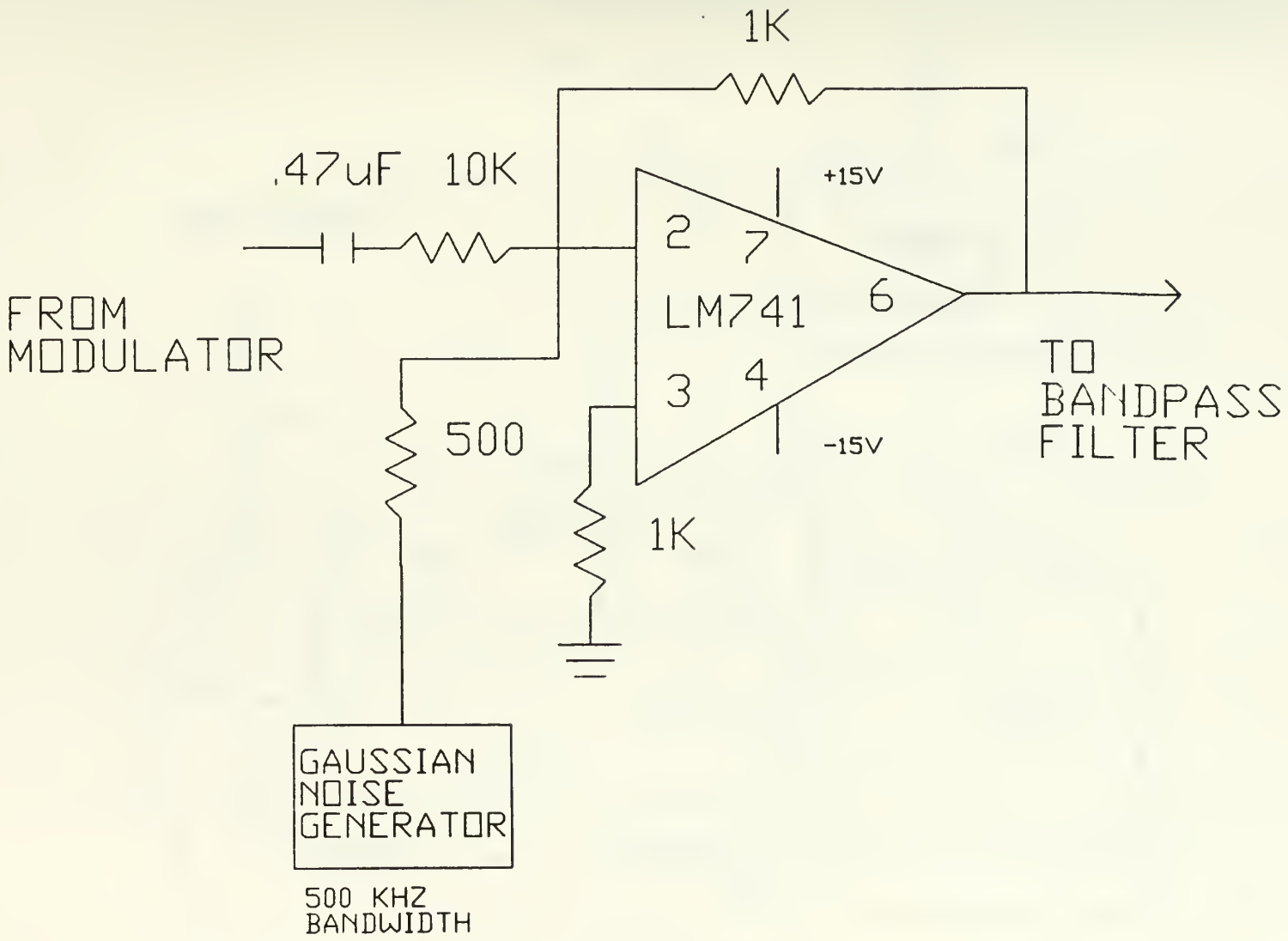


Fig. A-3. Channel.

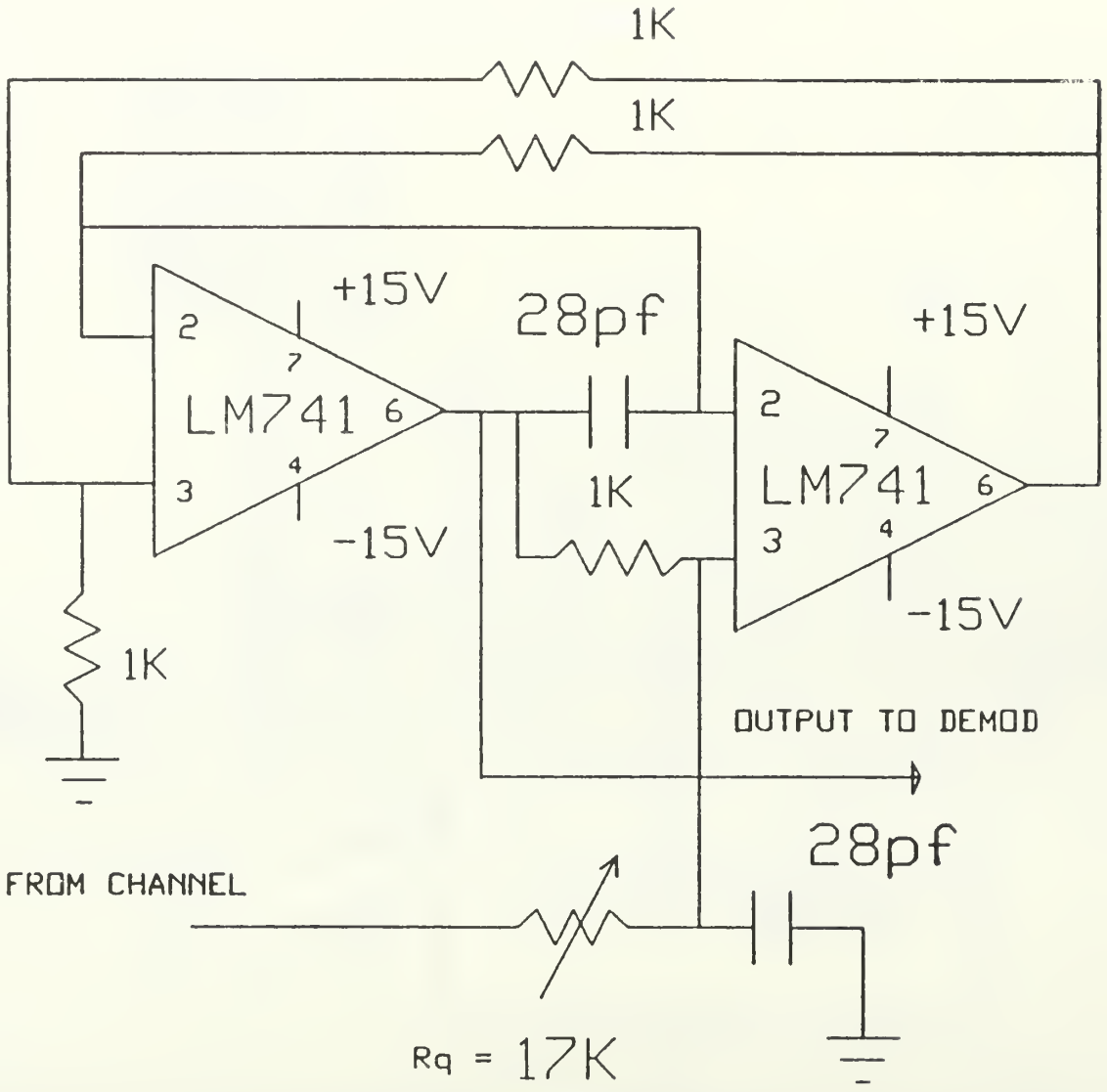


Fig. A-4. Bandpass Filter.

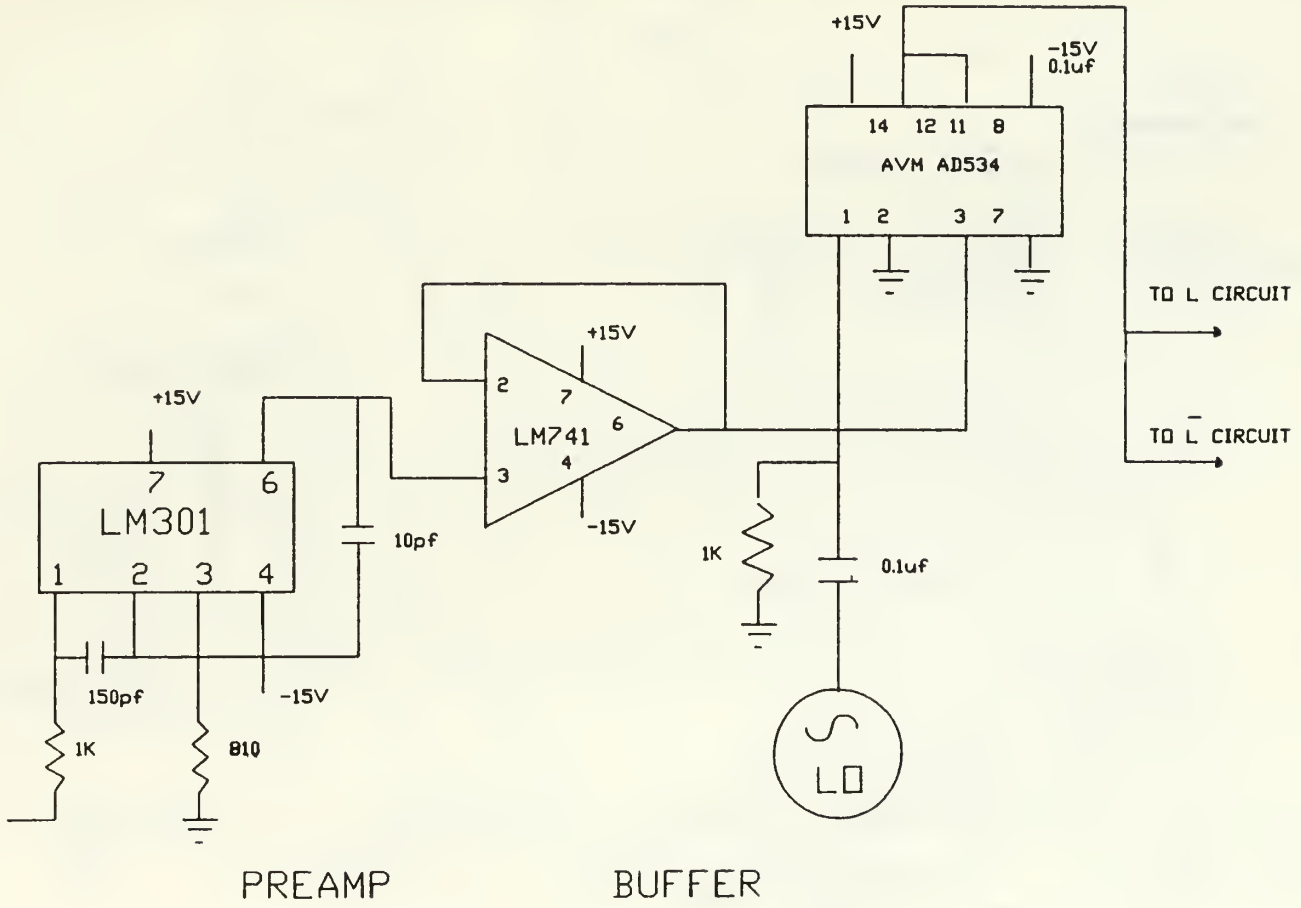


Fig. A-5. Demodulator Circuit.

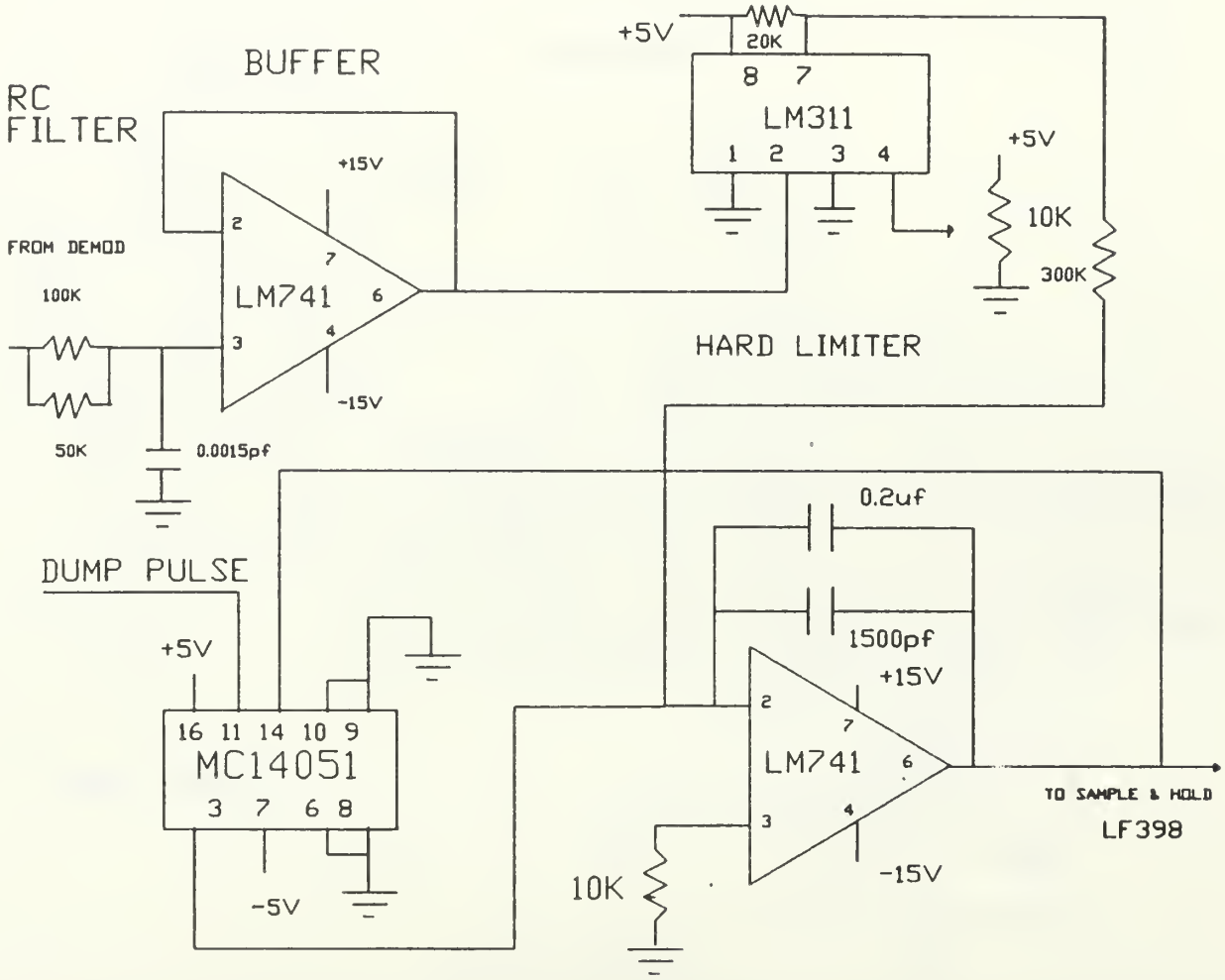
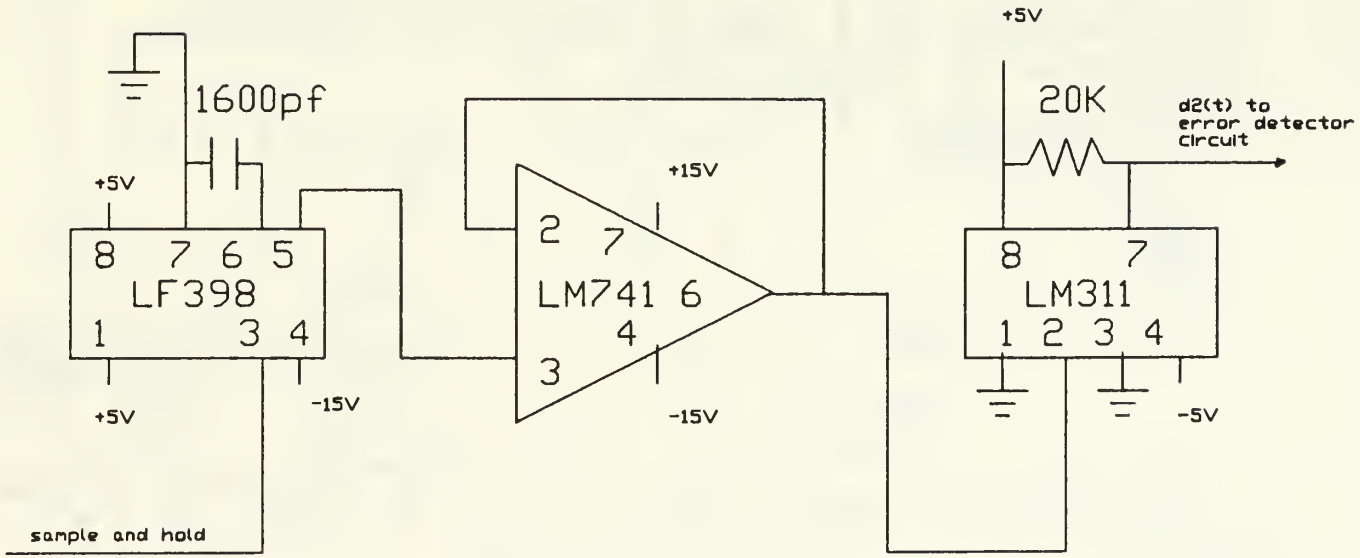


Fig. A-6a. Limiter Circuit.



BUFFER COMPARATOR

L DETECTOR

Fig. A-6b. Limiter Circuit.

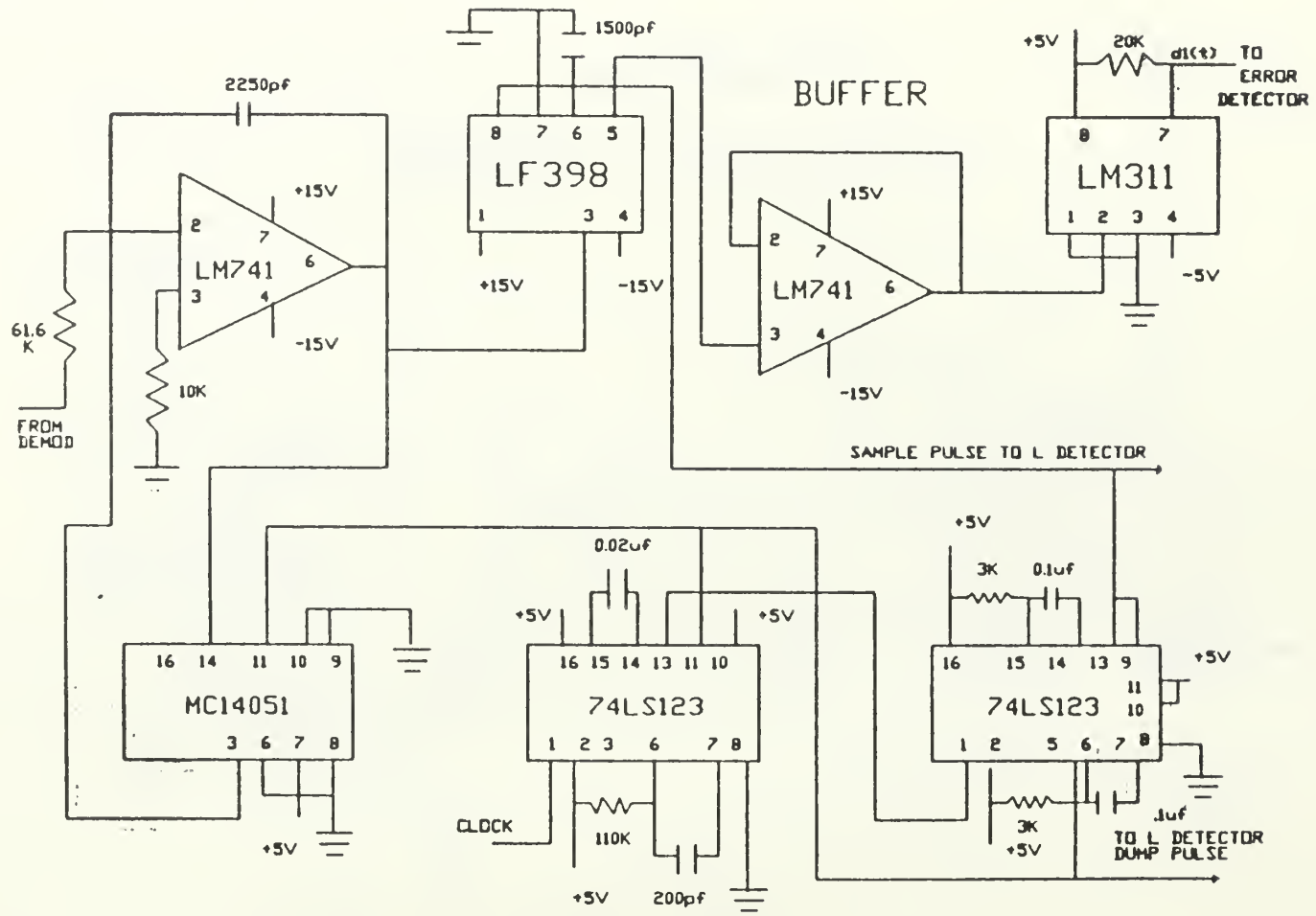


Fig. A-7. $\overline{L}$ Circuit.

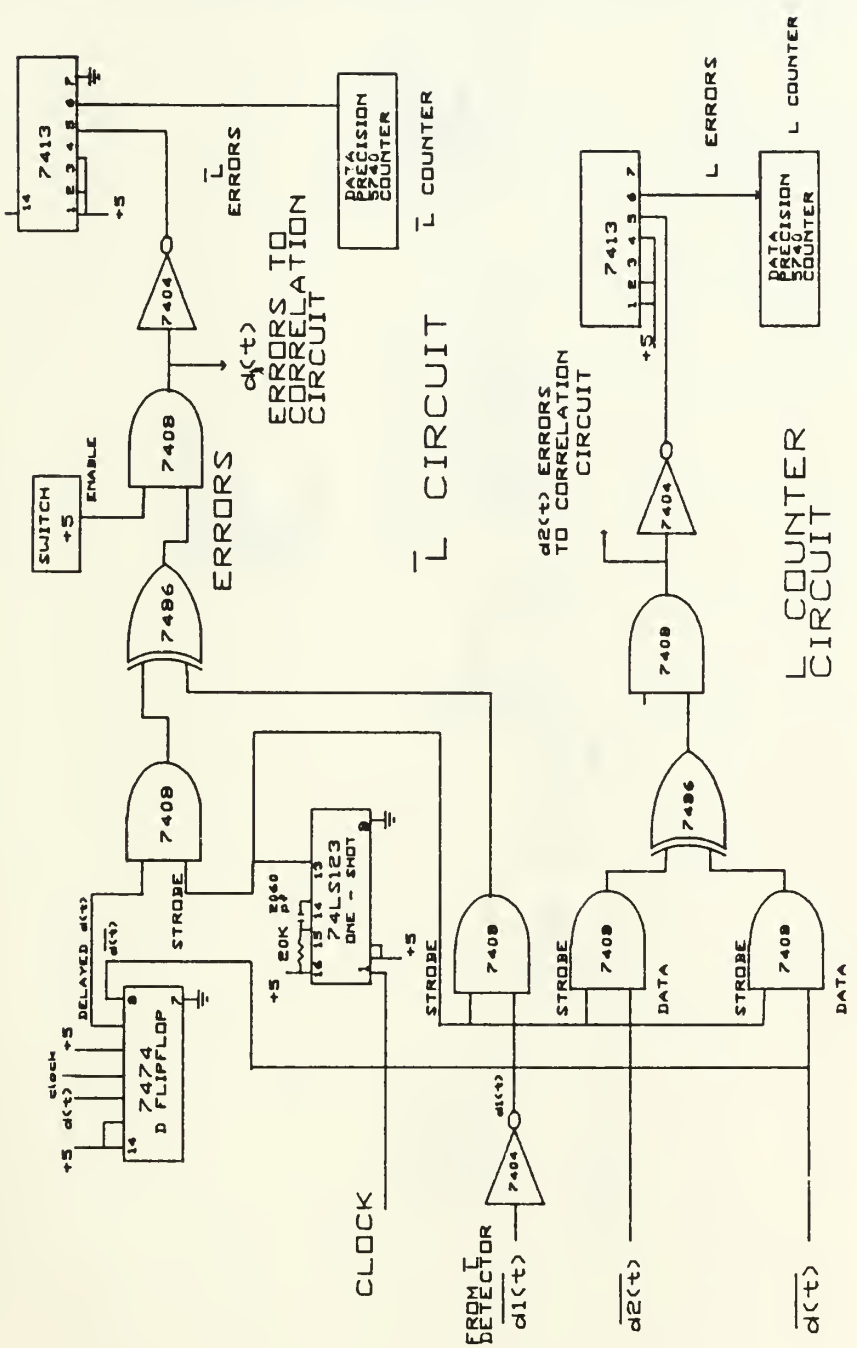


Fig. A-8. Error Detector.

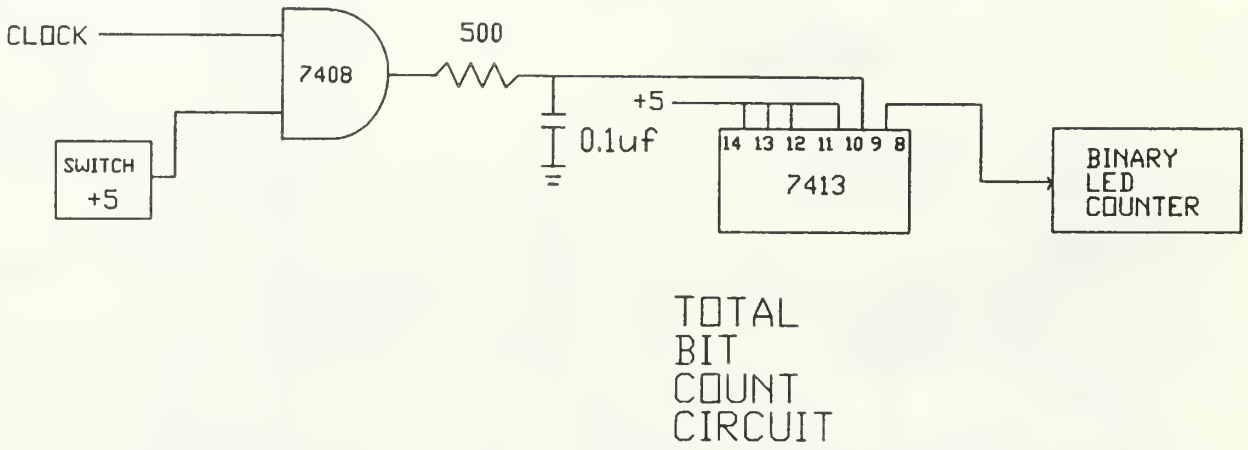


Fig. A-9. Total Bit Counter Circuit.

LIST OF REFERENCES

1. Feher, Kamilio, Digital Communications, Satellite Earth Station Engineering, Prentice Hall, 1981.

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